BMS INSTITUTE OF TECHNOLOGY AND MANAGEMENT
YELAHANKA – BANGALORE - 64
DEPARTMENT OF ELECTRONICS AND COMMUNICATION

Course code and title: **18EC42/Analog Circuits**	Course Credits: **(3:2:0) 4**
CIE: **40 Marks**	SEE: **60 Marks**
No. of Theory hours: **3+2 (Tut) per week**	
Course Coordinators: **Dr. Surekha.R.Gondkar/ Dr. M. C. Hanumantharaju**	Academic Year : **2019-20 EVEN**

Course Outcomes:

1. Understand the characteristics of BJTs and FETs
2. Design and analyze BJT and FET amplifier circuits.
3. Design sinusoidal and non-sinusoidal oscillators
4. Understand the functioning of linear ICs
5. Design of Linear IC based circuits

Syllabus/Course contents:

MODULE I

BJT Biasing: Biasing in BJT amplifier circuits: The Classical Discrete circuit bias (Voltage-divider bias), Biasing using a collector to base feedback resistor. Small signal operation and Models: Collector current and transconductance, Base current and input resistance, Emitter current and input resistance, voltage gain, Separating the signal and the DC quantities, The hybrid Π model. MOSFETs: Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor. Small signal operation and modeling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance. [Text 1: 3.5(3.5.1, 3.5.3), 3.6(3.6.1 to 3.6.6), 4.5(4.5.1, 4.5.2, 4.5.3), 4.6(4.6.1 to 4.6.6)]

MODULE II

MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance RS, Source follower. MOSFET internal capacitances and High frequency model: The gate capacitive effect, Junction capacitances, High frequency model. Frequency response of the CS amplifier: The three frequency bands, high frequency response, Low frequency response. Oscillators: FET based Phase shift oscillator, LC and Crystal Oscillators (no derivation) [Text 1: 4.7(4.7.1 to 4.7.4, 4.7.6) 4.8(4.8.1, 4.8.2, 4.8.3), 4.9, 12.2.2, 12.3.1, 12,3,2]

MODULE III

Feedback Amplifier: General feedback structure, Properties of negative feedback, The Four Basic Feedback Topologies, The series-shunt, series-series, shunt-shunt and shunt-series amplifiers (Qualitative Analysis). Output Stages and Power Amplifiers: Introduction, Classification of output stages,, Class A output stage, Class B output stage: Transfer Characteristics, Power Dissipation, Power Conversion efficiency, Class AB output stage, Class C tuned Amplifier. [Text 1: 7.1, 7.2, 7.3, 7.4.1, 7.5.1, 7.6 (7.6.1 to 7.6.3), 13.1, 13.2, 13.3(13.3.1, 13.3.2, 13.3.3, 13.4, 13.7)]

MODULE IV

Op-Amp with Negative Feedback and general applications Inverting and Non inverting Amplifiers – Closed Loop voltage gain, Input impedance, Output impedance, Bandwidth with feedback. DC and AC Amplifiers, Summing, Scaling and Averaging Amplifiers, Instrumentation amplifier, Comparators, Zero Crossing Detector, Schmitt trigger. [Text 2: 3.3(3.3.1 to 3.3.6), 3.4(3.4.1 to 3.4.5) 6.2, 6.5, 6.6 (6.6.1), 8.2, 8.3, 8.4]

MODULE V

Op-Amp Circuits: DAC - Weighted resistor and R-2R ladder, ADC- Successive approximation type, Small Signal half wave rectifier, Active Filters, First and second order low-pass and high-pass Butterworth filters, Band-pass filters, Band reject filters. 555 Timer and its applications: Monostable and Astable Multivibrators. [Text 2: 8.11(8.11.1a, 8.11.1b), 8.11.2a, 8.12.2, 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9, 9.4.1, 9.4.1(a), 9.4.3, 9.4.3(a)]

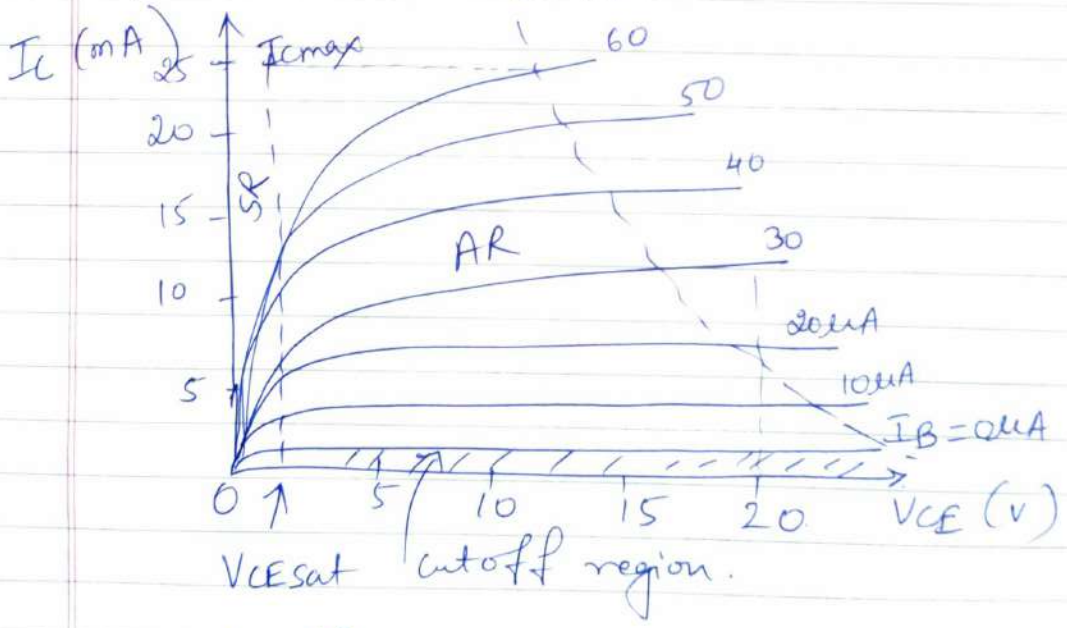
CONTENTS

MODULE 1

BJT Biasing in BJT amplifier circuits

The term biasing means the application of dc voltages to establish a fixed level of current and voltage For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is fixed on the characteristics it is also called quiescent (meaning quiet, still, inactive) point and is abbreviated as Q point. The biasing ckt can be designed to set the device at any operating point within the active region.

The following fig shows general O/p device characteristics.



cut off $I_B \leq 0\mu A$

Saturation $V_{CE} \leq V_{CEsat}$

Max power constraint is defined by the curve P_{cmax}.

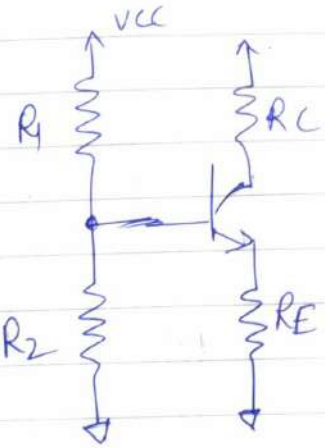
If the BJT is biased outside these max limits, then this will result in considerable shortening of the lifetime of the device or device destruction. So it is always desired to bias the BJT in the active region.

Once the transistor is biased at a desired operating point the effect of temp must also be considered. Temp causes the device parameters such as current gain (β_{ac}) and transistor leakage current (I_{CEO}) to change and thereby changes the operating point set by the biasing network. Therefore the biasing network must also provide temp stability. This maintainance of operating point can be specified by a stability factor S, which indicates the degree of change in operating point due to temp variation.

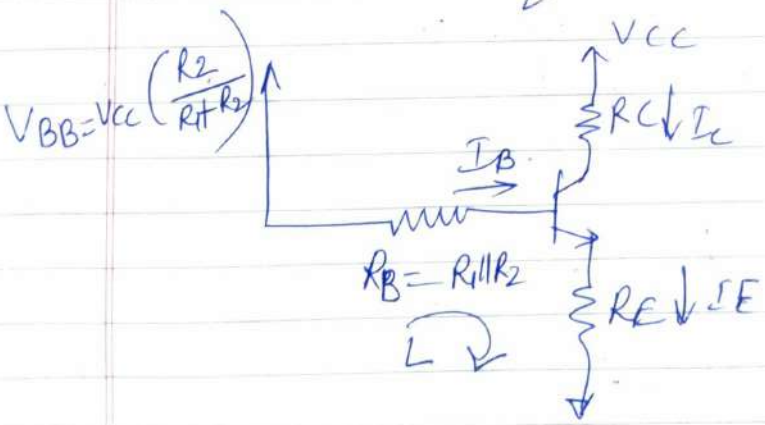
The biasing problem is that of establishing a constant dc current in the collector of the BJT. This current has to be calculable, predictable and insensitive to variations in temperature and to the large variations in the value of β encountered among transistors of the same type.
Another important consideration in bias region is locating the dc bias point in the $i_C - v_{CE}$ plane to allow for maximum output signal swing

The Classical Discrete-Circuit Bias Arrangement

The following fig shows the most commonly used for biasing a discrete-circuit transistor amplifier if only a single power supply is available. The technique consists of supplying the base of the transistor with a fraction of the supply voltage V_{CC} through the voltage divider R_1, R_2. In addition, a resistor R_E is connected to the emitter.



Following fig shows the same ckt with the voltage-divider network replaced by its thevenin equivalent.



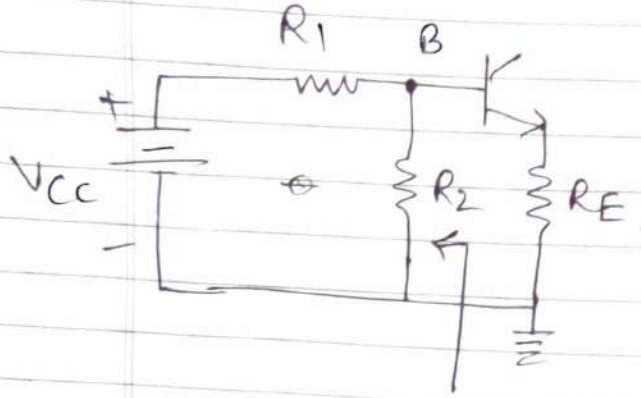
$$V_{BB} = \frac{R_2}{R_1+R_2} V_{CC} \quad \text{or } V_{Th} \qquad \text{——(1)}$$

$$R_B = \frac{R_1 R_2}{R_1+R_2} \quad \text{or } R_{Th} \qquad \text{——(2)}$$

The above equations are obtained as follows —

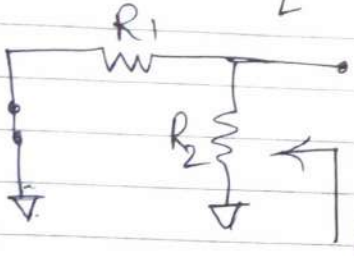
Boylestad

Consider the input side of the n/w shown below —



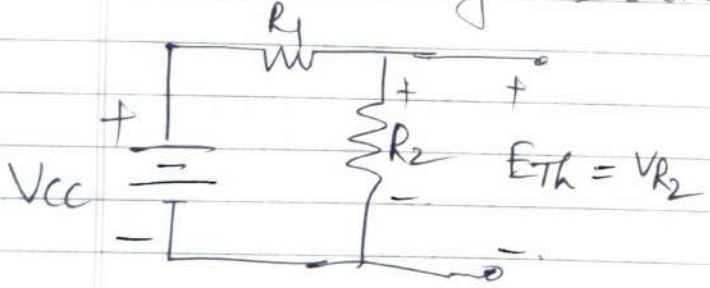
Thevenin

The voltage source is replaced by a short ckt eq as —



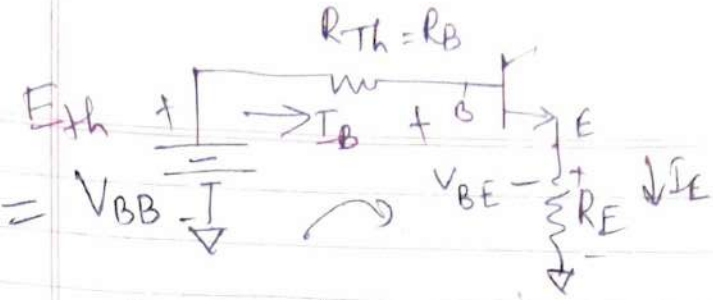
$$R_{Th} = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

The voltage source Vcc is returned to the network and the open-circuit Thevenin voltage is determined as follows.



$$E_{Th} = V_{R_2} = \frac{V_{cc} R_2}{R_1 + R_2}$$

The Thevenin network is then redrawn as shown —



By applying Kirchoff's voltage law to the loop we get

$$-E_{th} + R_{th} \cdot I_B + V_{BE} + R_E I_E = 0. \quad \text{—(1)}$$

Substituting $I_E = (\beta+1) I_B$ —(2)

$$R_{th} I_B + R_E(\beta+1) I_B = E_{th} - V_{BE}$$

$$\therefore \underset{\text{at q pt}}{I_B} = \frac{E_{th} - V_{BE}}{R_{th} + (\beta+1) R_E} \quad \text{—(3)}$$

OR. from (1)

$$\frac{I_E \cdot R_{th}}{\beta+1} + R_E I_E = E_{th} - V_{BE}$$

$$\underset{\text{at q pt}}{I_E} = \frac{E_{th} - V_{BE}}{\left(\frac{R_{th}}{\beta+1}\right) + R_E} \quad \text{—(4)} \;//$$

Once I_B is known, the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration.

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Sedra To make I_E insensitive to temperature and β variation, the ckt is designed to satisfy the following two constraints

V_{BB} & $E_{th} >> V_{BE}$ — (5).

& $R_E >> \frac{R_{th}(\&\, R_B)}{\beta+1}$ — (6).

Condition (5) ensures that small variations in V_{BE} ($\cong 0.7V$) will be swamped by the much larger V_{BB} (E_{th})
Condition (6) makes I_E insensitive to variations in β and could be satisfied by selecting R_B small. This in turn is achieved by using low values for R_1 & R_2. Lower values for R_1 and R_2, however will mean a higher current drain from the power supply and will result in a lowering of the input resistance of the amplifier, which is the trade-off involved in this part of the design.

EX 3.13 Design the bia network of the Sedra amplifier to establish a current $I_E = 1mA$; using a Power supply $V_{CC} = +12V$. The transistor is specified to have a nominal β value of 100.

Soln Rule of thumb — Choose one-third ($\frac{1}{3} V_{CC}$) of the supply vg to the vg drop across R_2. and another one-third vg drop across R_C leaving one-third for possible signal swing at the collector

16.1.

$$V_B = +4V$$

$$V_E = 4 - V_{BE} = 3.3V$$

$$R_E = \frac{V_E}{I_E} = \frac{3.3}{1mA} = 3.3k\Omega$$

Select a vg-divider current of
$0.1 I_E = 0.1 \times 1 = 0.1mA$

Neglecting the base current

$$R_1 + R_2 = \frac{12}{0.1m} = 120k\Omega \quad \text{---(1)}$$

$$\frac{R_2}{R_1+R_2} V_{cc} = 4V.$$

$12R_2 = 4R_1 + 4R_2$
$8R_2 = 4R_1$
$R_1 = 2R_2$
Substituting in (1).
$2R_2 + R_2 = 120k\Omega$
$R_2 = \frac{120k\Omega}{3}$
$R_2 = 40k\Omega$ $4R_1 = 2R$
$= 8$

Thus $R_2 = 40k\Omega$ $R_1 = 80k\Omega$

A more accurate I_E is estimated by taking into consideration the non-zero base current.

$$I_E = \frac{4 - 0.7}{3.3k + \left(\frac{80}{101}\right)k} = 0.93mA$$

(in Boot it is 80/40)

⇒ This is less than 1mA (given)

Thus choose $R_E = 3k\Omega$ which results in $I_E = 1.01mA \cong 1mA$

$$= \frac{333.3}{29.967 \times 10^3} \cdot \frac{(3.3)10^3}{(333.3 + 26.66)10^3}$$

$$= \frac{333.3}{359.96 \times 10^3} = 0.9259mA //$$

$R_E = 3k\Omega \cong 0.93mA \Rightarrow$
Results $I_E = 1.01mA \cong 1mA$

~~$R_1 = 8k\Omega$ $R_2 = 4k\Omega$ using initial $R_E = 3.3k$~~

~~$I_E = \frac{4 - 0.7}{3.3 + 0.027} = 0.99mA$~~

~~$I_C = \alpha I_E$~~
~~$0.99mA \cong 1mA$~~ ~~$R_C = \frac{12 - V_C}{I_C} = \frac{12 - 8}{1} = 4k\Omega$~~

If a lower i/p resistance for the amplifier resulting in drawing higher current from the power supply is acceptable then choose

$R_1 = 8k\Omega$ & $R_2 = 4k\Omega$.

with actual value of $3.3k\Omega$ for R_E (This is refered to as design-2

In this case $I_E = \dfrac{4-0.7}{3.3k + \dfrac{8k \| 4k}{\beta+1}}$

$R_{th} = R_1 \| R_2 = \dfrac{8\times10^3 \times 4\times10^3}{12\times10^3} = \dfrac{8}{3}$

$= \dfrac{8}{3} k\Omega = 2.66 k\Omega$.

$\therefore I_E = \dfrac{3.3}{3.3k + \dfrac{2.66\times10^3}{101}} = \dfrac{3.3\times101}{333.3\times10^3 + 2.66\times10^3}$

$= \dfrac{333.3}{335.96\times10^3}$

$= 0.992\ mA$.

$\cong 1\ mA$

Finally the value of R_C can be determined from

$R_C = \dfrac{12 - V_C}{I_C}$ $\{I_C \cong I_E\}$

$\beta = \dfrac{\alpha}{1-\alpha}$

$\alpha = \dfrac{\beta}{1+\beta}$

From the thumb rule drop across R_C is $\frac{1}{3}V_{CC}$ i.e $I_C R_C = 4V$.

$\therefore V_C = 8V$.

$\therefore R_C = \dfrac{12-8}{I_C} = \dfrac{4}{1mA}$.

$R_C = 4k\Omega$ //

Boyle.

$C_{in} = 10\mu F$ $C_{out} = 10\mu F$ $C_E = 50\mu F$.

Ex

$R_1 = 39k\Omega$ $R_C = 10k\Omega$ $V_{CC} = +22V$

$R_2 = 3.9k\Omega$ $R_E = 1.5k\Omega$.

$$R_{th} = R_1 \| R_2 = 3.55k\Omega$$

$$E_{th} = \frac{R_2 V_{CC}}{R_1 + R_2} = 2V$$

$$I_B = \frac{E_{th} - V_{BE}}{R_{th} + (\beta+1)R_E} = 8.05\mu A$$

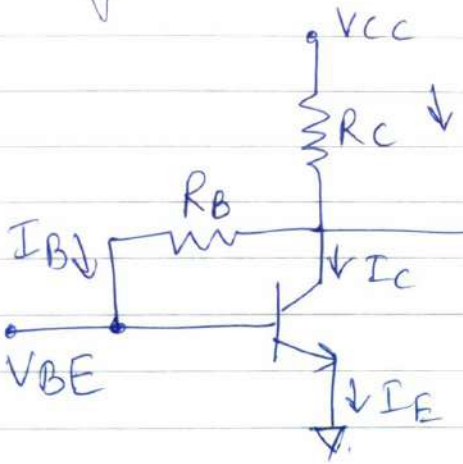
$$I_C = \beta I_B = 0.85mA$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

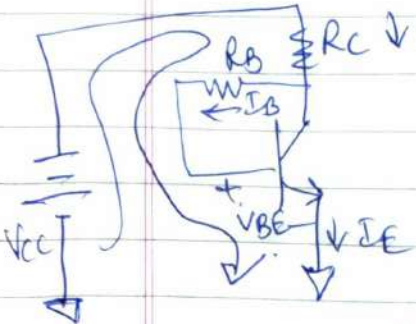
$$= 12.22V.$$

Biasing using a collector to Base Feedback Resistor.

Following fig shows a simple but effective alternative biasing arrangement suitable for common-emitter amplifiers. The ckt employs a resistor R_B connected between the collector and the base. Resistor R_B provides negative feedback, which helps to stabilize the bias point of the BJT. Although the Q point is not totally independent of β, the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed bias or a emitter-biased configurations.



From the fig, we can write.



$$-V_{CC} + R_C I_E + R_B I_B + V_{BE} = 0 \quad \text{---(1)}$$

$$-V_{CC} + R_C I_E + \frac{I_E}{\beta+1} R_B + V_{BE} =$$

$$I_E \left(R_C + \frac{R_B}{\beta+1} \right) = V_{CC} - V_{BE}.$$

$$\text{or } I_E = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta+1}} \quad \text{— (2)}$$

From (1) $\Rightarrow$

$$-V_{CC} + (\beta+1) R_C \cdot I_B + R_B I_B + V_{BE} = 0$$

$$I_B \left[R_C(\beta+1) + R_B \right] = V_{CC} - V_{BE}$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_C} \quad \text{— (3)}$$

If $I_E \cong I_C$

then $$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C} \quad \text{— (4)}$$

To obtain a value of I_E that is insensitive to variation of β, we select $\left(\frac{R_B}{\beta+1}\right) << R_C$ in eq^n (2)

Note however, that the value of R_B determines the allowable signal swing at the collector since

$$V_{CB} = I_B R_B = \frac{I_E R_B}{\beta+1} \quad \text{— (5)}$$

Ex Design the collector to base bias ckt to obtain a dc emitter current of 1mA and to ensure a ± 2V signal swing at the collector, that is, design for

$V_{CE} = +2.3V$. Let $V_{cc} = 10V$ and $\beta = 100$

$I_E = 1mA$ $V_{CB} = \pm 2V$ $V_{CE} = 2.3V$
$V_{CC} = 10V$ $\beta = 100$.

{ Since V_{CB} gives the allowable signal swing

we have $V_{CB} = I_B R_B = 2V$

$R_B = \frac{2}{I_B}$ }

$$R_C = \frac{V_{CC} - V_{CE}}{I_E}$$

$$= \frac{10 - 2.3}{1 \times 10^{-3}} = 7.7K\Omega$$ ✓

$R_C = 7.5k\Omega$
std value from chart

From (2) $\Rightarrow$

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta+1}}$$

$$= \frac{10 - 0.7}{7.7 \times 10^3 + \frac{R_B}{100+1}} = \frac{9.3 \times 101}{777.7K + R_B}$$

$$I_E = \frac{939.3}{777.7K + R_B}$$

$$777.7K + R_B = \frac{939.3}{1mA}$$

$$R_B = 939.3K - 777.7K$$

$$= 161.6k\Omega$$ (In book 162k ans)

std value $R_B = 160k\Omega$ (from chart)

Recalculating I_E from (2)

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{\beta+1}}$$

$$= \frac{10 - 0.7}{7.5k + \frac{160K}{100+1}}$$

$$= \frac{9.3}{7.5k + 1.584k}$$

$$= \frac{9.3}{9.084} \text{ mA}$$

$$= 1.02 \text{ mA}.$$

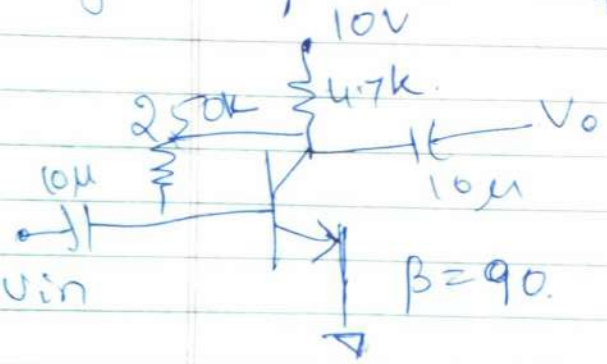
$$V_C = V_{CC} - I_E R_C$$

$$= 10 - 1.02 \times 10^{-3} \times 7.5 \times 10^{3}$$

$$= 10 - 7.65$$

$$= 2.35 \text{ V}.$$

Ex Determine the quiescent levels of I_{CQ} and V_{CEQ} for the n/w shown.



$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}$$

$$= 13.81 \mu A$$

$$I_{CQ} = \beta I_B = 1.24 \text{ mA}$$

$$V_{CEQ} = V_{CC} - I_C R_C$$

$$= 4.15 \text{ V}$$

or $V_{CEQ} = V_C$

$$= V_{BE} + I_B R_B$$

$$= 4.15 \text{ V}$$

Small signal operation and models

Consider the conceptual ckt shown in the following fig. Here the base-emitter junction is forward biased by a dc voltage V_{BE} (battery). The reverse bias of the collector-base junction is established by connecting the collector to another power supply of voltage V_{CC} through a resistor R_C. The input signal to be amplified is represented by the voltage source v_{be} that is superimposed on V_{BE}.

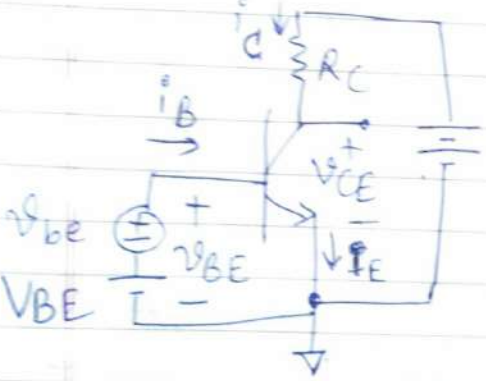


fig (a)

First consider the dc bias conditions by setting the signal v_{be} to zero. The ckt reduces to that shown below

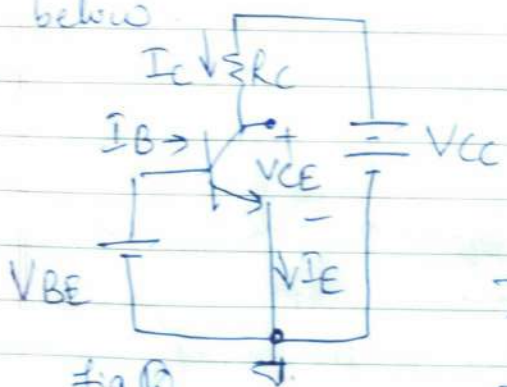


fig (b).

Following are the relationships for the dc currents and voltages

$$I_C = I_S e^{V_{BE}/V_T} \quad \text{---(1)}$$

$$I_E = I_C/\alpha \quad \text{---(2)}$$

$$I_B = I_C/\beta \quad \text{---(3)}$$

$$V_C = V_{CE} = V_{CC} - I_C R_C \quad \text{---(4)}$$

For active-mode, V_C should be greater than $(V_B - 0.4)$ by an amount that allows for a reasonable signal swing at the collector

NOTE

In the forward region the $i-v$ relationship is closely approximated by

$$i = I_S\left(e^{v/nV_T} - 1\right) \quad \text{— (1)}$$

Here I_S — saturation current & is constant for a given diode at a given temp. Another name is 'scale current'.

V_T is a constant called the thermal voltage and is given by

$$V_T = \frac{kT}{q} \quad \text{— (2)}$$

where

k = Boltzmann's constant $= 1.38 \times 10^{-23}$ Joules/kelvin

T = The absolute temperature in kelvins
$= 273 +$ temp in °C

q = The magnitude of electronic charge
$= 1.60 \times 10^{-19}$ coulomb.

For ckt analysis we use $V_T \simeq 25$ mV at room temp.

In the diode equation the constant n has a value 1 and 2, depending on the material and the physical structure of the diode.

For appreciable current i in the forward direction, specifically for $i \gg I_S$, eqn (1) can be approximated by the exponential relationship

$$i = I_S e^{v/nV_T} \quad \text{—(3)}$$

This relationship can be expressed alternatively in the logarithmic form

$$v = nV_T \ln \frac{i}{I_S} \quad \text{—(4)}$$

3.6.1 The collector current and the transconductance

If a signal v_{be} is applied as shown in fig (a), the total instantaneous base-emitter voltage v_{BE} becomes

$$v_{BE} = V_{BE} + v_{be}$$

Correspondingly the collector current becomes

$$i_C = I_S e^{v_{BE}/V_T}$$

$$= I_S e^{(V_{BE} + v_{be})/V_T}$$

$$= I_S e^{(V_{BE}/V_T)} \cdot e^{(v_{be}/V_T)}$$

Use of eqn (1) yields

$$i_C = I_C e^{v_{be}/V_T} \quad \text{——(5)}$$

Now if $v_{be} << V_T$ eqn (5) can be approximated as

$$i_C \cong I_C \left(1 + \frac{v_{be}}{V_T}\right) \quad \text{——(6)}$$

Here the exponential in eqn (5) is expanded in a series and retained only the first two terms. This approximation, which is valid only

for v_{be} less than approximately 10 mV is referred to as the "Small signal approximation". Under this approximation the total collector current is given by eq (6) and can be rewritten as —

$$i_C = I_C + \frac{I_C}{V_T} v_{be} \quad \text{—— (7)}$$

Thus the collector current is composed of the dc bias value I_C and a signal component i_c

$$i_c = \frac{I_C}{V_T} v_{be} \quad \text{—— (8)}$$

This equation relates the signal current in the collector to the corresponding base-emitter signal voltage. It can be rewritten as

$$i_c = g_m v_{be} \quad \text{—— (9)}$$

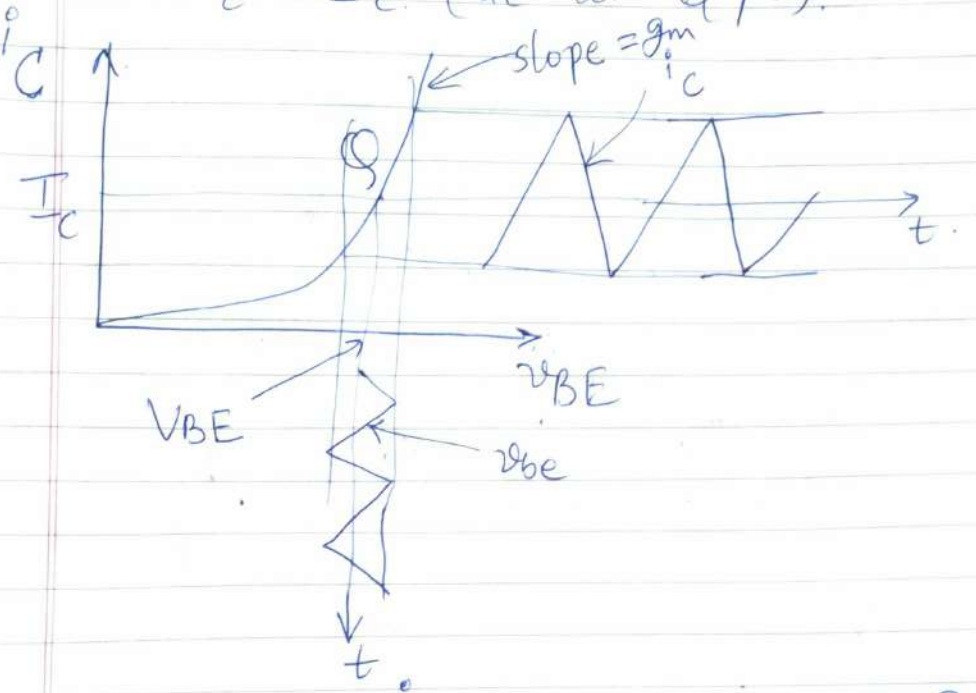
where g_m is called the "transconductance" and from eq (8) it is given by

$$\boxed{g_m = \frac{I_C}{V_T}} \quad \text{— (10)}$$

We observe that the transconductance of the BJT is directly proportional to the collector bias current I_C. Thus to obtain a constant predictable value for g_m, we need a constant predictable I_C. Finally note that

BJT's have relatively high transconductance as compared to MOSFETs

A graphical interpretation for g_m is given in following fig, where it is shown that g_m is equal to the slope of the $i_C - v_{BE}$ characteristic curve at $i_C = I_C$ (ie at Q pt).



Thus $g_m = \left.\frac{i_C}{v_{BE}}\right|_{i_C = I_C}$ ——— (11)

The small-signal approximation implies keeping the signal amplitude sufficiently small so that "operation" is restricted to an almost-linear segment of the $i_C - v_{BE}$ exponential curve.

The analysis above suggests that for small signals $v_{be} << V_T$, the transistor behaves as a voltage-controlled current source.

3.6.2 The Base Current and the Input Resistance at the base:

To determine the resistance seen by v_{be}, first evaluate the total base current i_B using eq^n (7)

ie $i_B = \frac{i_C}{\beta}$

$$= \frac{I_C}{\beta} + \frac{I_C}{\beta V_T} v_{be}$$

$$= I_B + i_b \quad \text{—— (12)}$$

where I_B is equal to I_C/β and the signal component i_b is given by

$$i_b = \frac{I_C}{\beta V_T} \cdot v_{be} \quad \text{—— (13)}$$

Substituting for I_C/V_T by g_m gives ——

$$i_b = \frac{g_m v_{be}}{\beta} \quad \text{— (14)}$$

The small signal input resistance between base and emitter, looking into the base, is denoted by r_π and is defined as

$$r_\pi = \frac{v_{be}}{i_b} \quad \text{—— (15)}$$

Using eq^n (14) we get

$$r_\pi = \frac{\beta}{g_m} \quad \text{— (16)}$$

Thus r_π is directly dependent on β and is inversely $\propto$ to the bias current I_C.

Substituting for g_m in eq (16) from eq^n (10)

$$r_\pi = \frac{\beta}{I_C / V_T}$$

$$= \frac{V_T}{I_C} \cdot \beta = \frac{V_T}{I_C/\beta} = \frac{V_T}{I_B} \quad \text{——— (17)}$$

3.6.3 The Emitter Current and the Input Resistance at the Emitter. ——

The total current i_E can be determined from —

$$i_E = \frac{i_C}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha}$$

$$i_E = I_E + i_e \quad \text{——— (18)}$$

where I_E is equal to I_C/α and the signal current i_e is given by

$$i_e = \frac{i_c}{\alpha} = \frac{I_C}{\alpha V_T} \cdot v_{be}$$

(from eq^n 8 $i_c = \frac{I_C}{V_T} v_{be}$)

$$i_e = \frac{I_E}{V_T} v_{be} \quad \text{——— (19)}$$

If we denote the small-signal resistance between base and emitter looking into the emitter, by r_e it can be defined as —

$$r_e \cong \frac{v_{be}}{i_e} \quad \text{---(20)}$$

Using eqn (19) we find that r_e, called the emitter resistance, is given by

$$r_e = \frac{V_T}{I_E} \quad \text{---(21)}$$

Comparing eqn (21) with (10)

$$r_e = \frac{V_T}{I_e/\alpha} = \alpha \frac{V_T}{I_C}$$

$$= \frac{\alpha}{g_m}$$

$$\cong \frac{1}{g_m} \quad \text{---(22)}$$

The relationship between r_π and r_e can be found by combining their respective definitions in eqns (15) and (20)

From (15) $v_{be} = r_\pi i_b$

From (20) $v_{be} = r_e i_e$

$\therefore \quad r_\pi i_b = r_e i_e$

$$r_\pi = \left(\frac{i_e}{i_b}\right) r_e = (\beta+1) r_e \quad \text{---(23)}$$

OR

$$r_e = \left(\frac{i_b}{i_e}\right) r_\pi$$

$$= \frac{r_\pi}{\beta+1}$$

Ex 3.37 A BJT having $\beta = 100$ is biased at a dc collector current of 1 mA. Find the value of g_m, r_e and r_π at the bias point.
[Ans: 40 mA/V, 25 Ω, 2.5 kΩ] given.

Soln Given $\beta = 100$

$I_C = 1\text{mA}$

$$g_m = \frac{I_C}{V_T}$$

$$V_T = \frac{kT}{q} = \frac{1.38 \times 10^{-23}}{1.60 \times 10^{-19}} \times T$$

Note: for ckt analysis we use $V_T \cong 25\text{ mV}$ at room temp.

$$\therefore g_m = \frac{1 \times 10^{-3}}{25 \times 10^{-3}}$$

$$= 0.04$$

$$= 40\text{ mA/V}.$$

From eqn (2a)

$$r_e \cong \frac{1}{g_m} = \frac{1}{40 \times 10^{-3}}$$

$$= 25\,\Omega$$

$$r_\pi = (\beta + 1)\, r_e$$

$$= (100 + 1)\, r_e$$

$$= 2525\,\Omega$$

$$\cong 2.5\text{ k}\Omega.$$

3.64 Voltage Gain

From previous topics it is shown that the transistor senses the base-emitter signal v_{be} and causes a α current $i_c = g_m \cdot v_{be}$ to flow in the collector lead at a high impedance level. In this way the transistor is acting as a voltage-controlled current source.

To obtain an output voltage signal, we may force this current to flow through a resistor, as shown in fig @.

The total collector voltage v_C will be —

$$v_C = V_{CC} - i_C R_C$$
$$= V_{CC} - (I_C + i_c) R_C$$
$$= (V_{CC} - I_C R_C) - i_c R_C \quad (24)$$
$$= V_C - i_c R_C$$

Here the quantity V_C is the dc bias voltage at the collector, and the signal voltage is given by

$$v_c = - i_c R_C = - g_m v_{be} R_C$$
$$= (- g_m R_C) v_{be} \quad — (25)$$

Thus the voltage gain of this amplifier A_v is —

$$A_v = \frac{v_c}{v_{be}} = - g_m R_C \quad — (26)$$

Here again we note that because g_m is directly $\propto$ to the collector bias current, the gain will be as stable as the collector bias current is made. Substituting for g_m, from eq^n (10) $\left[g_m = \frac{I_C}{V_T}\right]$ enables us to express the gain in the form

$$A_v = \frac{I_C R_C}{V_T} \quad \text{---} \quad (27)$$

{ which is identical to the ~~expression~~ large signal amplifier gain $A_v = -\frac{I_C R_C}{V_T} = -\frac{V_{RC}}{V_T}$

where $V_{RC} = V_{CC} - V_{CE}$ }

EX 3.38 In the ckt of fig @, V_{BE} is adjusted to yield a dc collector current of 1mA. Let $V_{CC} = 15V$. $R_C = 10k\Omega$ and $\beta = 100$. Find the voltage gain v_c/v_{be}. If $v_{be} = 0.005 \sin\omega t$ volts find $v_c(t)$ and $i_B(t)$.

[Ans: $-400 V/V$; $5 - 2\sin\omega t$ volts $10 + 2\sin\omega t\ \mu A$]

Given $I_C = 1mA$. $V_{CC} = 15V$ $R_C = 10k\Omega$

$\beta = 100$. $v_{be} = 0.005 \sin\omega t$.

$$g_m = \frac{I_C}{V_T} = \frac{1\times10^{-3}}{25\times10^{-3}} = 0.04.$$

$$A_v = \frac{v_c}{v_{be}} = -g_m R_C = -0.04 \times 10 \times 10^{3}$$

$$= -400\ V/V.$$

$$v_c(t) = (-g_m R_C)\, v_{be}$$

$$= -400 \times 0.005 \sin\omega t$$

$$= -2\sin\omega t.$$

$$V_C = V_{CC} - I_C R_C$$

$$= 15 - 1\times10^{-3} \times 10\times10^{3}$$

$$= 5\,V.$$

$$\therefore v_C = V_C + v_c$$

$$= 5 - 2\sin\omega t.$$

$$i_B = I_B + i_b.$$

$$i_b = \frac{I_C}{\beta V_T} v_{be}.$$

$$= \frac{1\times10^{-3}}{100 \times 25\times10^{-3}} \times 0.005\sin\omega t$$

$$= 0.000002\sin\omega t = 2\sin\omega t\,\mu A$$

$$I_B = \frac{I_C}{\beta} = \frac{1\times10^{-3}}{100} = 10^{-5}$$

$$= 10\,\mu A.$$

$$\therefore i_B = (10 + 2\sin\omega t)\,\mu A$$

3.6.5 Separating the Signal and the DC Quantities —

The analysis above indicates that every current and voltage in the amplifier ckt of fig (a) is composed of two components; a dc component and a signal component.

The dc components are determined from the dc ckt given in fig (b). On the other hand, a representation of the signal operation of the BJT can be obtained by eliminating the dc sources as shown in the following fig (c).

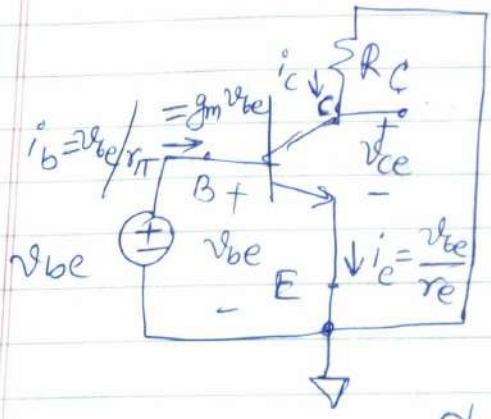


fig (c)

Observe that since the voltage of an ideal dc supply doe not change, the signal voltage across it will be zero. For this reason, VCC & VBE are replaced by short ckts. Had the ckt contained ideal dc current sources, these would have been replaced by open ckts.

Note however that the ckt of fig (c) is useful only in so far as it shows the various signal currents and voltages. It is not actual amplifier ckt since the dc bias ckt is not shown.

The fig also shows the expressions for the current increments (i_c, i_b and i_e) obtained when a small signal v_{be} is applied. These relationships can be represented by a ckt. Such a ckt should have three terminals - C B and E and should yield the same terminal currents indicated in fig ©. The resulting ckt is then equivalent to the transistor as far as small signal operation is concerned. and thus it can be considered an equivalent small signal ckt model

3.6.6 The Hybrid- π Model

An equivalent ckt model for the BJT is shown in the following fig. (d).

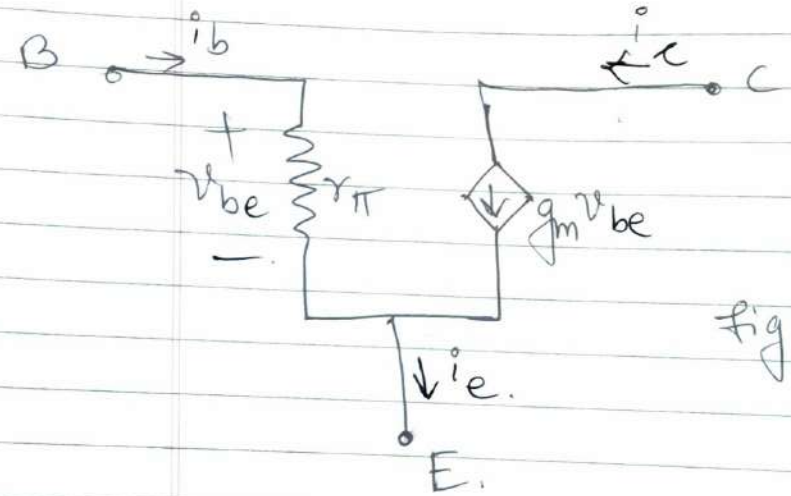


fig (d).

This model represents the BJT as a voltage-controlled current source and explicitly includes the input resistance looking into the base r_π. The model obviously yields

$$i_c = g_m v_{be}.$$

$$i_b = \frac{v_{be}}{r_\pi}.$$

The model also yields the current expression for i_e. This can be shown as follows —

At the emitter node we have

$$i_e = \frac{v_{be}}{r_\pi} + g_m v_{be}$$

$$= \frac{v_{be}}{r_\pi}(1 + g_m r_\pi)$$

From eqn (16) $r_\pi = \frac{\beta}{g_m}$

$$\text{or } \beta = r_\pi \cdot g_m$$

$$\therefore i_e = \frac{v_{be}}{r_\pi}(1+\beta)$$

$$= \frac{v_{be}}{\left(\frac{r_\pi}{1+\beta}\right)}$$

$$= \frac{v_{be}}{r_e}$$

{ From (23) $r_e = \frac{r_\pi}{\beta+1}$

A slightly different equivalent ckt model can be obtained by expressing the current of the controlled source ($g_m v_{be}$) in terms of the base current i_b as follows —

$$g_m v_{be} = g_m (i_b r_\pi)$$

$$= (g_m r_\pi) i_b$$

$$= \beta i_b$$

{ from eqn (15) $r_\pi = \frac{v_{be}}{i_b}$

This results in the alternate equivalent ckt model shown in the fig (e).

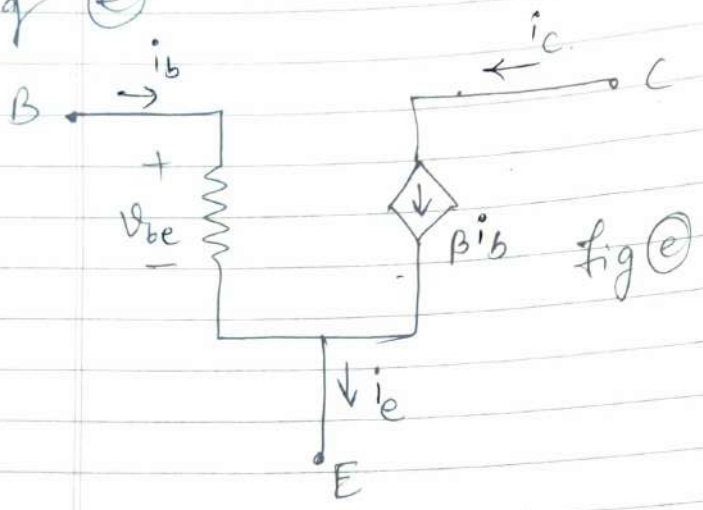


fig (e)

Here the transistor is represented as a current-controlled current source with the control current being i_b.

The two models in fig (d) & (e) are simplified versions of what is known as the hybrid π model. This is the most widely used model for the BJT.

Finally although the models have been developed for an npn transistor, they apply equally well to a pnp transistor with no change of polarities.

4.5 Biasing in MOS Amplifier Circuits

An essential step in the design of a MOSFET amplifier ckt is the establishment of an appropriate dc operating point for the transistor. This is the step known as biasing or bias design. A dc operating point or bias point is characterized by a stable and predictable dc drain current I_D and by a dc drain-to-source voltage V_{DS} that ensures operation in the saturation region for all expected input-signal levels.

Biasing by Fixing V_{GS}

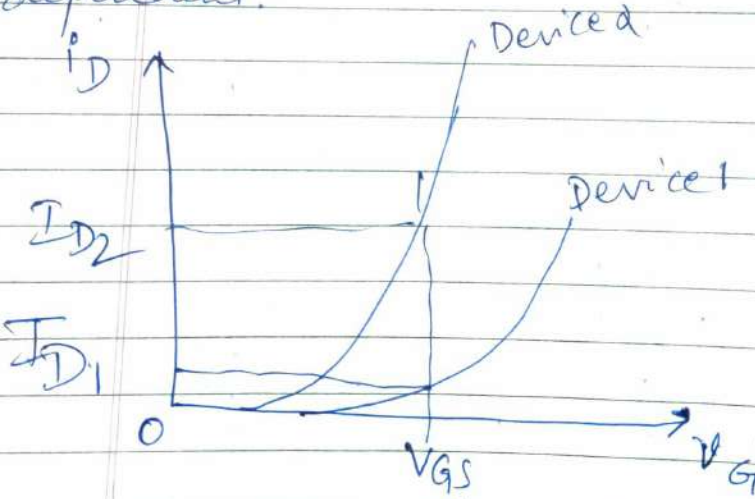
The most straightforward approach to biasing a MOSFET is to fix its gate to source voltage V_{GS} to the value required to provide the desired I_D. This voltage value can be derived from the power supply voltage V_{DD} through the use of an appropriate voltage divider. Alternatively it can be derived from another suitable reference voltage that might be available in the system.

Independent of how the voltage V_{GS} may be generated, this is not a good approach to biasing a MOSFET. To understand the reason for this statement, recall that

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2$$

μ_n – is the mobility of electrons in the channel called surface mobility. Its value depends on the fabrication process technology and note that the values of the threshold voltage V_t, the oxide-capacitance C_{ox}, and the transistor aspect ratio W/L vary widely among devices of the same size and type.

This is certainly the case for discrete devices, in which large spreads in the values of these parameters occur among devices of the same manufacturer's part number. The spread is also large in integrated ckts espicially among devices fabricated on different wafers and certainly between different batches of wafers. Furthermore, both V_t and μ_n depend on temperature with the result that if we fix the value of V_{GS}, the drain current I_D becomes very much temperature dependent.

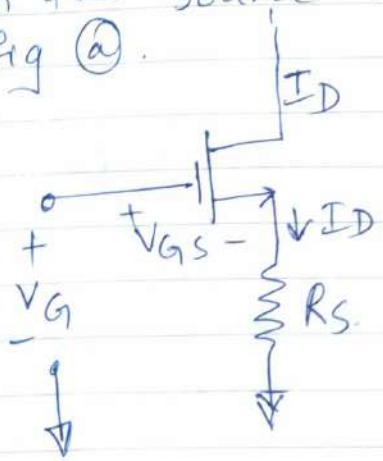


To emphasize the point that biasing by fixing V_{GS} is not a good technique, in the ~~graphs~~ fig

two $i_D - V_{GS}$ characteristic curves representing extreme values in a batch of MOSFETS of the same type. Observe that for the fixed value of V_{GS} the resultant spread in the values of the drain current can be substantial.

4.5.2 Biasing by Fixing V_G and connecting a Resistance in the Source —

An excellent biasing technique for discrete MOSFET circuits consists of fixing the dc voltage at the gate, V_G, and connecting a resistance in the source lead as shown in the fig (a).



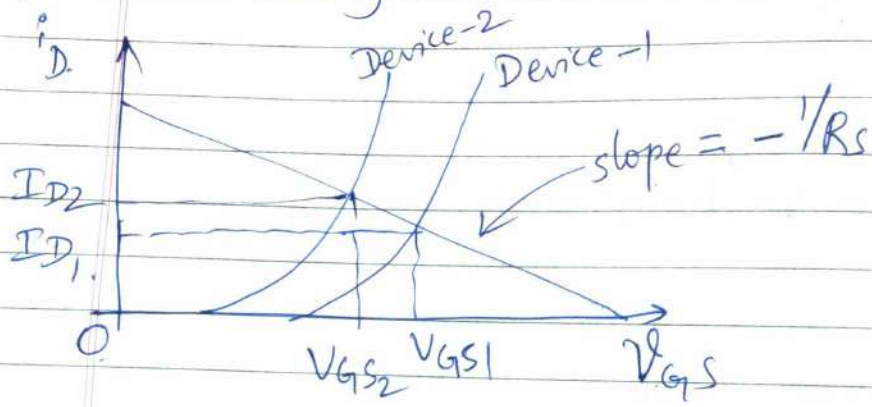
For this ckt we can write

$$V_G = V_{GS} + R_S I_D \quad \text{——— (1)}$$

Now, if V_G is much greater than V_{GS}, I_D will be mostly determined by the values of V_G and R_S. However even if V_G is not much larger than V_{GS}, resistor R_S provides -ve feedback, which acts to stabilize the value of the bias current I_D.

To see how this comes about consider the case when I_D increases for whatever reason. Eqn (1) indicates that since V_G is constant V_{GS} will have to decrease. This in turn results in a decrease in I_D, a change that is opposite to that initially assumed. Thus the action of R_S works to keep I_D as constant as possible. This -ve feedback action of R_S gives it the name "degeneration resistance".

Following fig (6) provides a graphical illustration of the effectiveness of this biasing scheme.



Here, the $i_D - v_{GS}$ chars for two devices that represent the extremes of a batch of MOSFETs are shown. Superimposed on the device chars is a straightline that represents the constraint imposed by eqn (1). The intersection of this straight line with the $i_D - v_{GS}$ char curve provides the coordinates (I_D and V_{GS}) of the bias point.

Observe that compared to the case of fixed V_{GS}, here the variability obtained in I_D is much smaller. Also note that variability decreases as V_G and R_S are made larger.

Two possible practical circuit implementations of this bias scheme are given here. [fig (c) & (d)]

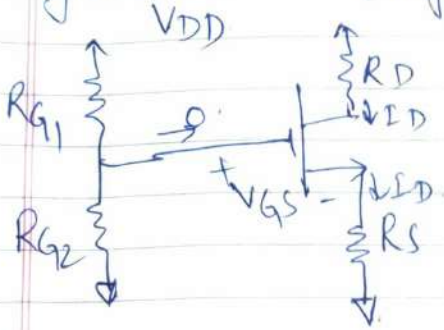


fig (c)

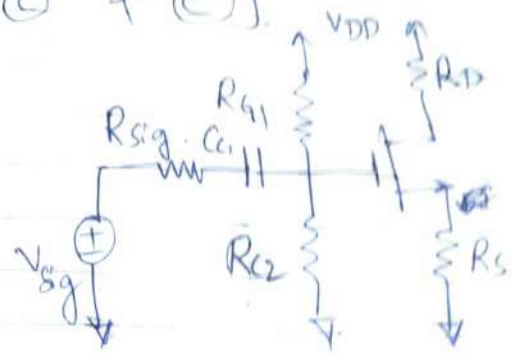
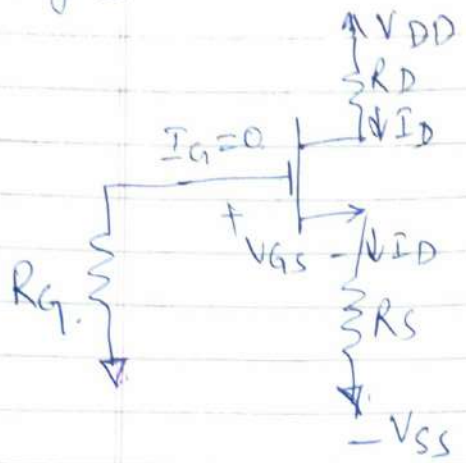


fig (d)

The ckt in fig (c) uses one power supply V_{DD} and derives V_G thro' a vg divider (R_{G1}, R_{G2}). Since $I_G = 0$, R_{G1} and R_{G2} can be selected to be very large (in the MΩ range), allowing the MOSFET to present a large input resistance to a signal source that may be connected to the gate thro' a coupling capacitor as shown in fig (d). Here C_{c1} blocks dc and allows to couple the signal V_{sig} to the amplifier input without disturbing the MOSFET dc bias point. It should be selected as large as possible so that it approximates a short ckt at all signal freqs of interest. The resistor R_D is selected to be as large as possible to obtain

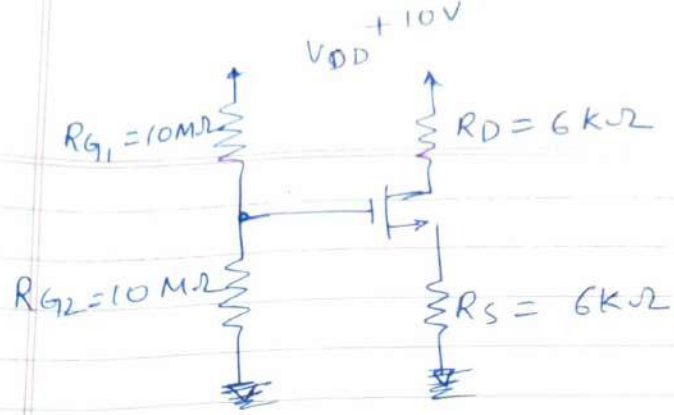
high gain but small enough to allow for the desired signal swing at the drain while keeping the MOSFET in saturation at all times.

When two power supplies are available, a simpler bias arrangement as shown in following fig (e) can be utilized.



This ckt is an implementation of eqn (1) with V_G replaced by V_{SS}. Resistor R_G establishes a dc ground at the gate and presents a high input resistance to a signal source that may be connected to the gate through a coupling capacitor.

EX Analyse the ckt shown in following fig to determine the voltages at all nodes and the currents through all branches.
Let $V_t = 1V$ and $k_n'(W/L) = 1mA/V^2$
Neglect the channel-length modulation effect (ie assume $\lambda = 0$)

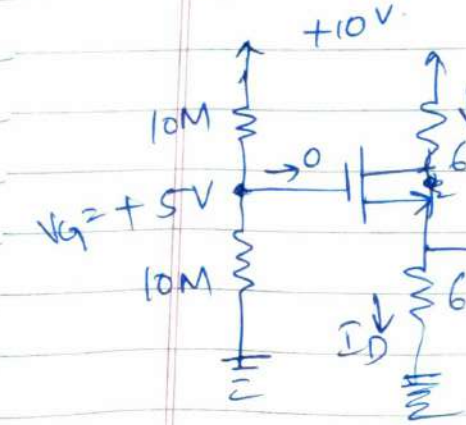


Since the gate current is zero, the V_g at the gate is simply determined by the voltage divider formed by the two 10 MΩ resistors

$$V_g = VDD \cdot \frac{R_{G2}}{R_{G1}+R_{G2}} = 10 \times \frac{10\times10^6}{(10+10)10^6}$$

$$= +5\ V$$

With this +ve V_g at the gate, the NMOS transistor will be turned on.
We do not know however, whether the transistor will be operating in the saturation region or in the triode region (ohmic region).
We shall assume saturation region operation & solve the problem & then check the validity of our assumption. Obviously, if our assumption turns out not to be valid, then we will have to solve the problem again for triode region operation.



V_g at source

$= 6\times10^3 \times I_D \times 10^{-3}$

$= 6I_D$.

$\{\because I_D$ is in mA

We have

$V_{GS} = V_G - 6I_D$

$= 5 - 6I_D.$

I_D is given by

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$$

$$= \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2$$

$$= \frac{1}{2} \times (4 - 6I_D)^2$$

$$= \frac{1}{2} [16 + 36I_D^2 - 2 \times 24 I_D]$$

$$= 8 + 18 I_D^2 - 24 I_D$$

$$I_D = 18 I_D^2 - 24 I_D + 8$$

Thus $18I_D^2 - 25I_D + 8 = 0$.

This yields two values for I_D ie 0.89mA & 0.5mA

when $I_D = 0.89mA$

Vg at source $= 6 \times 0.89 = 5.34V$

This is greater than the gate Vg (which is +5V). and does not make physical sense as it would imply that the NMOS transistor is cut off.

Thus $I_D = 0.5mA$.

& Vg at source $V_S = 0.5 \times 6 = +3V$

$V_{GS} = 5 - 3 = 2V$

$V_D = 10 - 6 \times 0.5 = +7V$

Since $V_D > V_G - V_t$, the transistor is operating in saturation as initially assumed.

Ex 4.9 Design the ckt shown in fig (c) to establish a dc drain current $I_D = 0.5mA$. The MOSFET is specified to have $V_t = 1V$ and $k_n' \frac{W}{L} = 1 mA/V^2$. For simplicity, neglect the channel-length modulation effect (ie assume $\lambda = 0$). Use a power supply $V_{DD} = 15V$. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same $k_n' \frac{W}{L}$ but $V_t = 1.5V$.

Soln As a rule of thumb for designing this biasing ckt R_D & R_S are selected such that one-third of power supply vg V_{DD} as a drop across each of R_D, the transistor (ie V_{DS}) and R_S.

For $V_{DD} = +15V$, this choice makes

$V_S = +5V$

$V_D = +10V$

Since $I_D = 0.5mA$ (Given).

$$R_D = \frac{V_{DD} - V_D}{I_D}$$

$$= \frac{15 - 10}{0.5 \times 10^{-3}}$$

$$= 10k\Omega$$

$$\& \; R_S = \frac{V_S}{I_D} = \frac{5}{0.5 \times 10^{-3}} = 10k\Omega.$$

The required value of V_{GS} can be determined by first calculating the overdrive vg V_{OV} from,

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{OV}^2$$

Note $k_n' = \mu_n C_{ox}$ is known as the process transconductance parameter as it determines the value of the MOSFET transconductance & has the dimensions of A/V^2.

Recall that in the MOSFET the gate and the channel region form a parallel plate capacitor for which the oxide layer serves as a dielectric If the capacitance per unit gate area is denoted by C_{ox} and the thickness of the oxide layer is t_{ox} then

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad [F/m^2 \text{ or } F/\mu m^2]$$

where ϵ_{ox} is the permittivity of the silicon oxide.

$$\epsilon_{ox} = 3.9\epsilon_0 = 3.9 \times 8.854 \times 10^{-12}$$
$$= 3.45 \times 10^{-11} \text{ F/m.}$$

The oxide thickness t_{ox} is determined by the process technology used to fabricate the MOSFET. (In nm)

$$0.5 = \frac{1}{2} \times 1 \times V_{OV}^2$$

$$\therefore V_{OV} = 1V.$$

Thus $V_{GS} = V_{OV} + V_t$.
$= 1 + 1$
$= 2V$

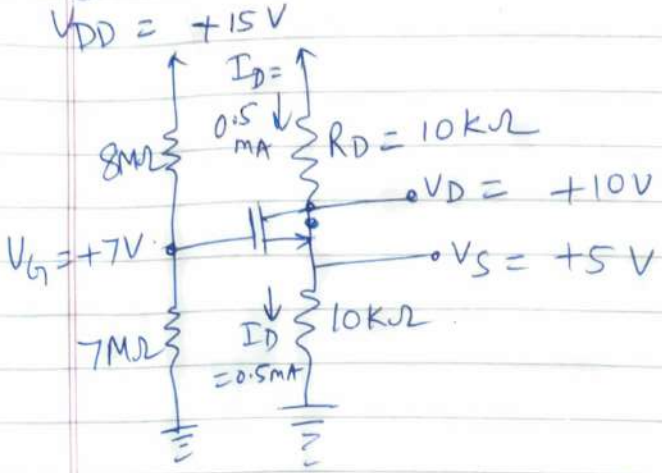
Sin $V_S = +5V$

$$V_G = V_S + V_{GS} = 5 + 2 = 7V$$

$$V_G = \frac{V_{DD} \cdot R_{G2}}{R_1 + R_2}$$

$$7 = \frac{15 R_{G2}}{R_{G1} + R_{G2}} \quad \text{—— (1)}$$

To establish this voltage at the gate we may select $R_{G1} = 8\,M\Omega$ & $R_{G2} = 7\,M\Omega$. The final ckt is shown below.



If the NMOS transistor is replaced by another having $V_t = 1.5V$, the new value of I_D can be found as follows:

$$I_D = \frac{1}{2} \times 1 \times (V_{GS} - 1.5)^2 \quad \text{—— (1)}$$

$$V_G = V_{GS} + I_D \cdot R_S$$

$$7 = V_{GS} + 10 I_D \quad \text{—— (2)}$$

$$V_{GS} = 7 - 10 I_D$$

(1) $\Rightarrow$

$$I_D = \frac{1}{2}\left[7 - 10 I_D - 1.5\right]^2$$

$$= \frac{1}{2}\left[5.5 - 10 I_D\right]^2$$

$$= \frac{1}{2}[$$

$I = 0.455\ mA.$

Thus the change in I_D is

$$\Delta I_D = 0.455 - 0.5$$
$$= -0.045\ mA.$$

which is $\dfrac{-0.045}{0.5} \times 100$

$= -9\%$ change //

4.5.3 Biasing Using a Drain to Gate Feedback Resistor

A simple and effective discrete circuit biasing arrangement utilizing a feedback resistor connected between the drain and the gate is shown in the following ckt.

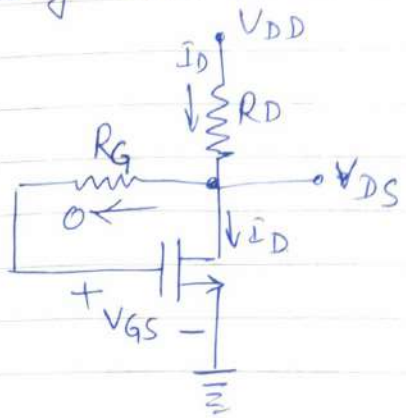


fig @

Here the large feedback resistance R_G (usually in the MΩ range) forces the dc voltage at the gate to be equal to that at the drain (Because $I_G = 0$).

Thus we can write

$$V_{GS} = V_{DS} = V_{DD} - R_D \cdot I_D$$

which can be rewritten in the form

$$V_{DD} = V_{GS} + R_D I_D. \quad \text{——— (1)}$$

Here also if I_D for some reason changes, say increases, then eqn (1) indicates that V_{GS} must decrease. The decrease in V_{GS} in turn causes a decrease in I_D, a change that is opposite in direction to the one originally assumed. Thus the -ve feedback or degeneration provided by R_G works to keep the value of I_D as constant as possible.

The ckt of fig @ can be utilized as an amplifier by applying the i/p vg signal to the gate via a coupling capacitor so as not to disturb the dc bias conditions already established.

This ckt has the drawback of a rather limited o/p vg swing.

Ex 4.2] It is required to design the ckt of fig ① to operate at a dc drain current of 0.5mA. Assume $V_{DD} = +5V$, $k_n' W/L = 1 mA/V^2$, $V_t = 1V$ and $\lambda = 0$. Use a std 5% resistance value for R_D and give the actual values obtained for I_D & V_D

Soln

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{ov}^2$$

$$0.5 \times 10^{-3} = \frac{1}{2} \times 1 \times 10^{-3} \times V_{ov}^2$$

$$V_{ov} = 1V.$$

$$V_{ov} = V_{GS} - V_t$$

$$\therefore V_{GS} = V_{ov} + V_t$$

$$= 1 + 1.$$

$$= 2V.$$

$$V_D = V_{GS} = 2V.$$

$$\therefore R_D = \frac{V_{DD} - V_D}{I_D}$$

$$= \frac{5 - 2}{0.5 \times 10^{-3}} = \frac{6}{\frac{30}{5 \times 10^{-3}}}$$

$$= 6 k\Omega.$$

Std value $= 6.2 k\Omega$

$$I_D = \frac{V_{DD} - V_D}{R_D} =$$

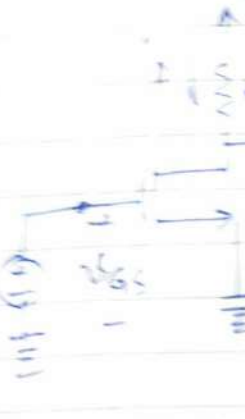
$$= 0.49 mA$$

$$V_D = V_{DD} - I_D \cdot R_D =$$

$$= 1.96V.$$

Signal Operation and Models

To this a conceptual common-source amplifier circuit shown below is considered.



Here the MOS transistor is biased by applying a dc voltage V_{GS}, a clearly impractical arrangement but one that is simple and useful for our purposes. The i/p signal to be amplified v_{gs} is shown superimposed on the dc bias voltage V_{GS}. The o/p v_d is taken at the drain.

The DC Bias Point:

The dc bias current I_D can be found by setting the signal v_{gs} to zero. Thus

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 \quad \text{——— (1)}$$

where the channel-length modulation is neglected (i.e assume $\lambda = 0$)

The dc voltage at the drain V_{DS} is simply V_D will be

$$V_D = V_{DD} - R_D I_D \quad \text{——— (2)}$$

To ensure saturation-region operation, we must have

$$V_D > V_{GS} - V_t$$

Furthermore, since the total voltage at the drain will have a signal component

superimposed on V_D, V_D has to be sufficiently greater than $(V_{GS} - V_t)$ to allow for the required signal swing.

4.6.2 The Signal Current in the Drain Terminal:

Consider the situation with the i/p signal v_{gs} applied. The total instantaneous gate-to-source voltage will be

$$v_{GS} = V_{GS} + v_{gs} \quad \text{—— (1)}$$

resulting in a total instantaneous drain current i_D

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t + v_{gs})^2$$

$$= \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 + k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs} + \frac{1}{2} k_n' \frac{W}{L} v_{gs}^2 \quad \text{—— (2)}$$

The first term is the dc bias current I_D. The second term represents a current component that is directly $\propto$ to the i/p signal v_{gs}. The third term is a current component that is $\propto$ to the square of the input signal. This last component is undesirable because it represents nonlinear distortion. To reduce the nonlinear distortion introduced by the MOSFET, the i/p signal should be kept small so that

$$\frac{1}{2} k_n' \frac{W}{L} v_{gs}^2 \ll k_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$$

resulting in

$$v_{gs} \ll 2(V_{GS} - V_t) \quad \text{——(3)}$$

OR equivalently

$$v_{gs} \ll 2V_{ov} \quad \text{——(4)}$$

where V_{ov} is the overdrive voltage at which the transistor is operating

If this 'small-signal condition' is satisfied, we may neglect the last term in eqn (1) and express i_D as

$$i_D = I_D + i_d \quad \text{——(4)}$$

where

$$i_d = k_n' \frac{W}{L}(V_{GS} - V_t) v_{gs}$$

The parameter that relates i_d and v_{gs} is the MOSFET 'transconductance' g_m

$$g_m = \frac{i_d}{v_{gs}} = k_n' \frac{W}{L}(V_{GS} - V_t) \quad \text{——(5)}$$

Or in terms of overdrive voltage V_{ov}

$$g_m = k_n' \frac{W}{L} V_{ov} \quad \text{——(6)}$$

Following fig shows a graphical interpretation of the small-signal operation of the enhancement MOSFET amplifier. Note that g_m is equal to the slope of the $i_D - v_{GS}$ char at the bias point

$$g_m = \left.\frac{i_D}{v_{GS}}\right|_{v_{GS} = V_{GS}} \quad \text{——(7)}$$

This is the formal definition of g_m, which can be shown to yield the expressions given in eqns (5) & (6).

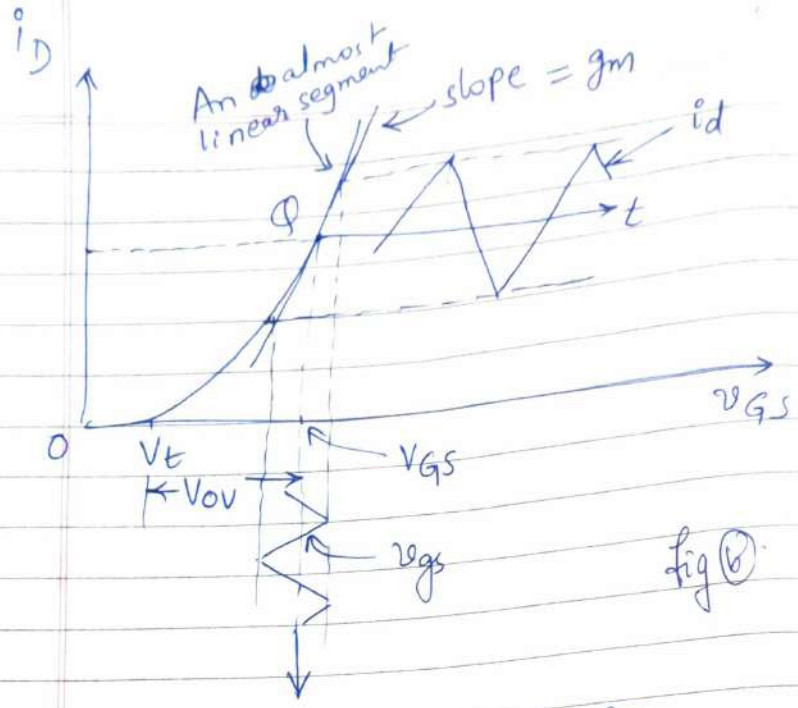


fig (b)

4.6.3 The Voltage Gain

From ckt in in fig (a), the total instantaneous drain voltage v_D is expressed as follows:

$$v_D = V_{DD} - R_D i_D$$

Under the small-signal condition we have: $v_D = V_{DD} - R_D(I_D + i_d)$

which can be rewritten as

$$v_D = V_D - R_D i_d$$

Thus the signal component of the drain voltage is

$$v_d = -i_d R_D$$

$$= -g_m v_{gs} \cdot R_D \quad \text{——(8)}$$

which indicates that the voltage gain is given by

$$A_v = \frac{v_d}{v_{gs}} = -g_m R_D \quad \text{——(9)}$$

The minus sign in eq^n (9) indicates that the output signal v_d is 180° out of phase with respect to the input signal v_{gs}. This is illustrated in the following fig (c)

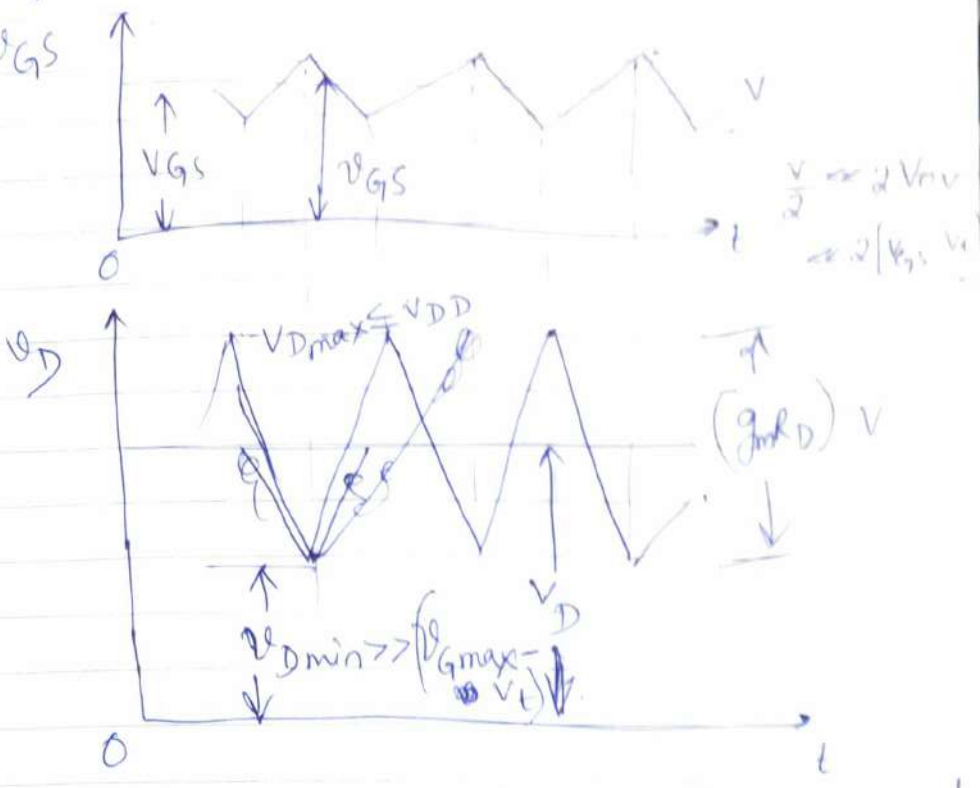


fig (d)

The input signal is assumed to have a triangular waveform with an amplitude much smaller than $2(V_{GS} - V_t)$, the small signal condition in eq^n (3), to ensure linear operation. For operation in the saturation region at all times, the minimum value of v_D should not fall below the corresponding value of v_G by more than V_t. Also the maximum value of v_D should be smaller than V_{DD}; Otherwise the FET will enter the cutoff region and the peaks of the output signal waveforms will be clipped off.

4.6.4 Seperating the DC Analysis and the Signal Analysis

From the previous analysis, it is observed that under the small signal approximation, signal quantities are superimposed on dc quantities.

It follows that the analysis and design can be greatly simplified by seperating dc or bias calculations from small-signal calculations. That is once a stable dc operating point has been established and all dc quantities calculated we may then perform signal analysis ignoring dc quantities.

4.6.5 Small-Signal Equivalent Circuit Models

From a signal point of view the FET behaves as a voltage-controlled current source. It accepts a signal v_{gs} between gate and source and provides a current $g_m v_{gs}$ at the drain terminal. The i/p resistance of this controlled source is very high - ideally infinite. The o/p resistance - that is, the resistance looking into the drain - also is high & it is assumed to be ∞ so far. Putting all of this together, we arrive at the ckt shown in fig below which represents the small-signal

operation of the MOSFET and is thus a small-signal model or a small-signal equivalent circuit

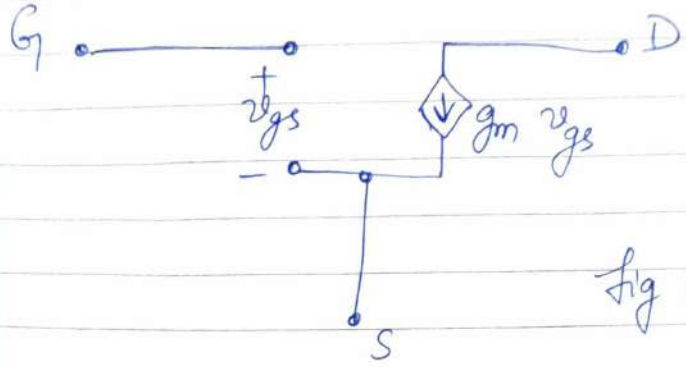


fig (a).

In the analysis of a MOSFET amplifier circuit, the transistor can be replaced by the equivalent circuit model shown in fig (a). The rest of the ckt remains unchanged except that ideal constant dc vg sources are replaced by short ckts. and an ideal dc current source can be replaced by an open ckt in the small signal equivalent ckt of the amplifier.

The most serious shortcoming of the small-signal model of fig (a) is that it assumes the drain current in saturation is independent of the drain voltage. But from the MOSFET characteristics in saturation, the drain current depend on v_{DS} in a linear manner. Such dependence was modeled by a finite resistance r_o between drain and source. which is given by

$$r_o = \frac{|V_A|}{I_D} \quad \text{—(1)}$$

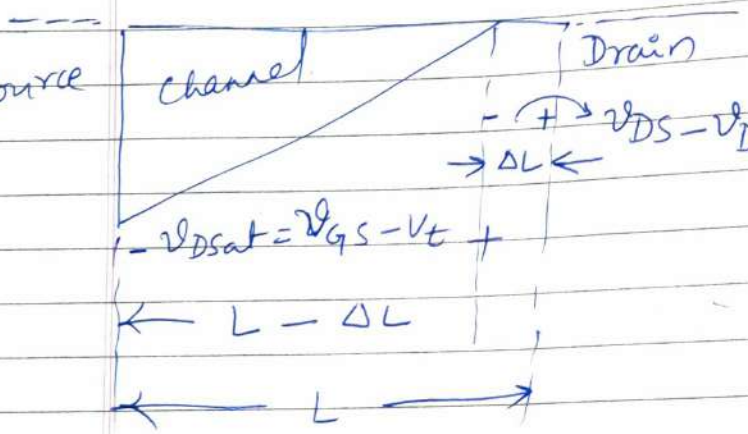
where

$$V_A = \frac{1}{\lambda}$$ a MOSFET parameter

that either is specified or can be measured. It is called as the Early voltage. For a given process tech, V_A is $\propto$ to the MOSFET channel length.

{{ Note $\lambda = \frac{\lambda'}{L}$ Dimensions V^{-1}

where λ' is a process technology parameter with the dimensions of $\mu m/V$, & L is the channel length between source & drain



The drain current considered so far

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

$$= \frac{1}{2} k_n' \frac{W}{L} V_{OV}^2 \quad \left| \text{ & } i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - \right.$$

$$= \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t +$$

indicate that in saturation, i_D is independent of v_{DS}. Thus a change Δv_{DS} in the drain to source vg causes a zero change in i_D, which implies that the incremental resistance looking into the drain of a saturated MOSFET is ∞. This however is an idealization based on the premise that once the channel is pinched off at the drain end, further increases in v_{DS} have no effect on the channel's

shape. But in practice, increasing v_{DS} beyond v_{DSsat} does affect the channel. Specifically, as v_{DS} is increased, the channel pinch-off point is moved slightly away from the drain, toward the source. This is illustrated in above fig from which it can be noted that the v_d across the channel remains constant at $v_{GS} - V_t = v_{DSsat}$ and the additional voltage applied to the drain appears as a voltage drop across the narrow depletion region between the end of the channel and the drain region. This voltage accelerates the electrons that reach the drain end of the channel and sweeps them across the depletion region into the drain. Note however that with depletion-layers widening, the channel length is in effect reduced, from L to L-ΔL, a phenomenon known as channel-length modulation. Now since i_D is inversely related to the channel length i_D increases with v_{DS}.

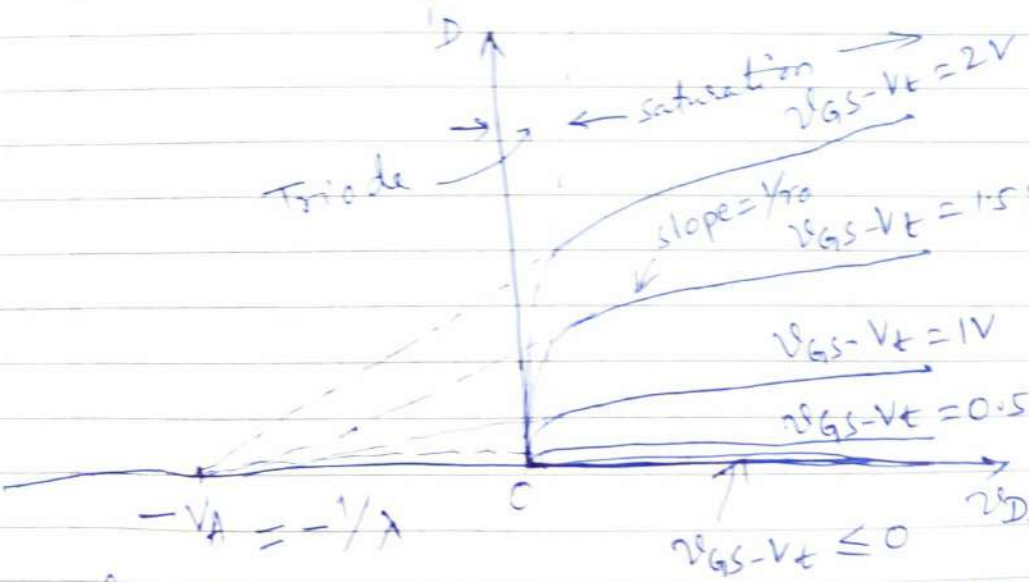


fig: Effect of v_{DS} on i_D in the saturation region.

The current I_D is the value of the dc drain current without the channel-length modulation taken into account; that is

$$I_D = \frac{1}{2} k_n' \frac{W}{L} V_{ov}^2 \quad \text{—— (2)}$$

Typically, r_o is in the range of 10 KΩ to 1000 KΩ.

It follows that the accuracy of the small signal model can be improved by including r_o in ||l with the controlled source as shown in fig (e)

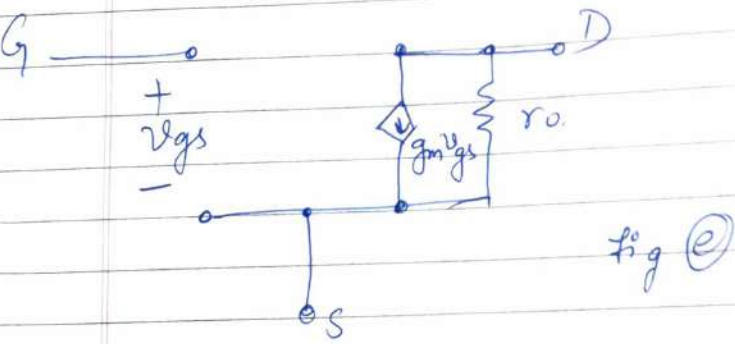


fig (e)

Note that the small signal model parameters g_m and r_o depend on the dc bias point of the MOSFET.

Replacing the MOSFET with the small-signal model of fig (e) in amp^r ckt of fig (a) results in the v_g gain expression

$$A_v = \frac{v_d}{v_{gs}}$$

$$= -g_m(R_D \| r_o) \quad \text{—— (3)}$$

Thus the finite o/p resistance r_o results in a reduction in the magnitude of the v_g gain

Although the above analysis is for NMOS transistor, the results and the equivalent ckt models apply equally well to PMOS devices, except for using $|V_{GS}|$, $|V_t|$, $|V_{ov}|$, and $|V_A|$ and replacing k_n' with k_p'.

4.6.6 The Transconductance g_m:

The MOSFET transconductance is given by

$$g_m = \frac{i_d}{v_{gs}}$$

$$= k_n' \left(\frac{W}{L}\right)(V_{GS} - V_t)$$

$$= k_n' \left(\frac{W}{L}\right) V_{ov} \quad \text{---(1)}$$

This relationship indicates that g_m is $\propto$ to the process transconductance parameter $k_n' = \mu_n C_{ox}$ and to the $\frac{W}{L}$ ratio of the MOS transistor; Hence to obtain relatively large transconductance the device must be short and wide.

Also observe that g_m is $\propto$ to the overdrive voltage $V_{ov} = V_{GS} - V_t$, the amount by which the bias voltage V_{GS} exceeds the threshold voltage V_t. Note however, that increasing g_m by biasing the device at a larger V_{GS} has the disadvantage of reducing the allowable voltage signal swing at the drain.

Another useful expression for g_m can be obtained by substituting for $(V_{GS} - V_t)$ in eqn (1)

We have

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(V_{GS} - V_t)^2$$

$$\therefore V_{GS} - V_t = \sqrt{2 I_D / k_n' \left(\frac{W}{L}\right)}$$

$$\therefore g_m = k_n' \left(\frac{W}{L}\right) \sqrt{\frac{2 I_D}{k_n' \left(\frac{W}{L}\right)}}$$

$$= \sqrt{k_n' \left(\frac{W}{L}\right) \cdot 2 I_D}$$

$$= \sqrt{2 k_n'} \sqrt{W/L} \sqrt{I_D} \quad \text{— (2)}$$

This expression shows that —

(1) For a given MOSFET, g_m is $\propto$ to the square root of the dc bias current

(2) At a given bias current, g_m is $\propto$ to $\sqrt{W/L}$

This is in contrast to transconductance of BJT which is $\propto$ to bias current & is independent of the physical size and geometry of the device

Yet another expression for g_m of the MOSFET can be obtained by substituting for $k_n'(W/L)$ by $2 I_D / (V_{GS} - V_t)^2$

ie $$g_m = \frac{2 I_D}{(V_{GS} - V_t)^2} \cdot (V_{GS} - V_t)$$

$$= \frac{2 I_D}{V_{GS} - V_t} \quad \text{— (3)}$$

In summary, there are 3 different relationships for determining g_m Eq? ①, ②, ③ and there are 3 design parameters — (W/L), V_{OV} and I_D, any two of which can be chosen independently. That is the designer may choose to operate the MOSFET with a certain overdrive voltage V_{OV} and at a particular current I_D; the required (W/L) ratio can then be found & the resulting g_m determined.

MODULE 2 : MOSFET AMPLIFIER CONFIGURATIONS

Basic MOSFET Amplifier configuration

3 'A' & 'B'

Basic configurations

① common source amplifiers : (CS) (fig a)

→ The source terminal is connected to ground.

→ The i/p voltage v_i is applied between the gate & ground and the o/p voltage signal v_o is taken between the drain and ground, across the resistance R_D.

→ It is most popular voltage amplifier. (shown in fig (a))

② common gate amplifiers (CG) : (fig (b))

→ Here, gate terminal is grounded.

→ i/p is applied between source and ground and o/p is taken across R_D connected between drain & gnd

→ CG amplifier has excellent high frequency response.

③ Common Drain amplifier (CD) : (fig (c)).

→ Here drain is grounded. I/p is applied between gate and ground. ~~o/p~~ The o/p is taken between the source and ground across a load resistance R_L.

fig (a) : CS

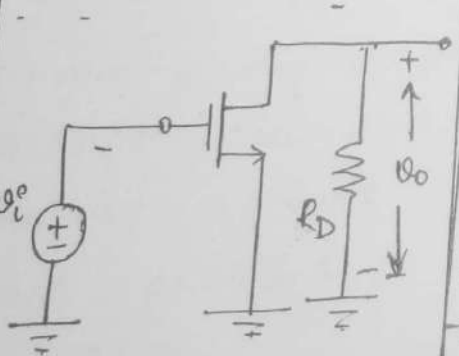


fig (b) : CG

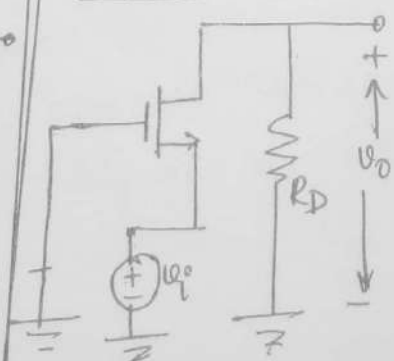
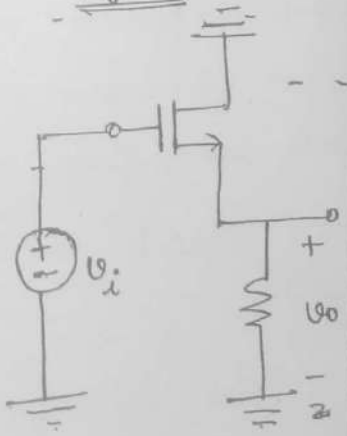
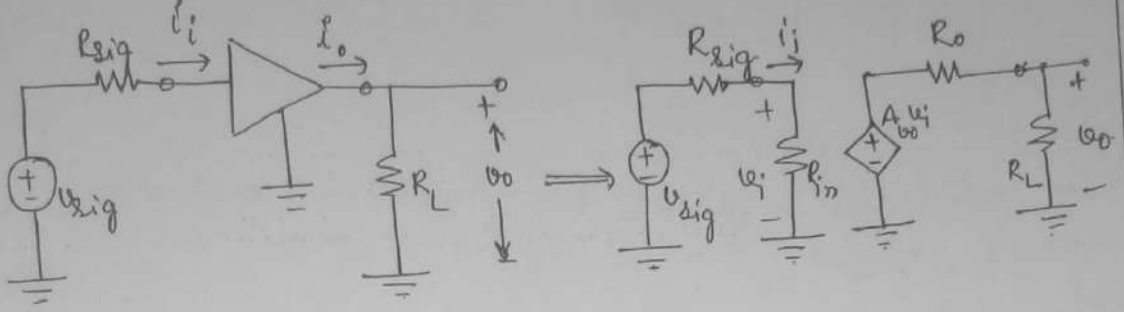


fig (c) : CD



Characterising Amplifiers:

The basic amplifier circuit with R_{sig} & R_L is as shown below.



→ $R_{in} = v_i / i_i$ where $v_i = v_{sig} \times \frac{R_{in}}{R_{in} + R_{sig}}$ ——— (1)

→ A_{vo} is open loop voltage gain i.e, when $R_L = \infty$

$$\boxed{A_{vo} = \left.\frac{v_o}{v_i}\right|_{R_L = \infty}}$$

→ $v_o = A_{vo} v_i \times \frac{R_L}{R_L + R_o}$ ——— (2)

{ where R_o is the resistance seen looking back into the amplifier o/p with $v_i = 0$ }

$$\therefore \boxed{A_v = \frac{v_o}{v_i} = A_{vo} \times \frac{R_L}{R_L + R_o}} \quad \text{——— (3)}$$

→ **Overall Voltage gain (G_v)**

$$G_v = \frac{v_o}{v_{sig}}$$

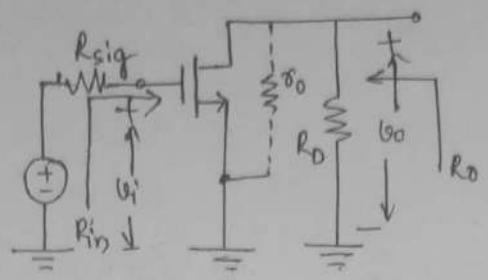
from (1) & (2)

$$G_v = \frac{A_{vo} v_i \times \frac{R_L}{R_L + R_o}}{v_i \times \frac{(R_{in} + R_{sig})}{R_{in}}} = \frac{R_{in}}{R_{in} + R_{sig}} \times A_{vo} \times \frac{R_L}{R_L + R_o}$$

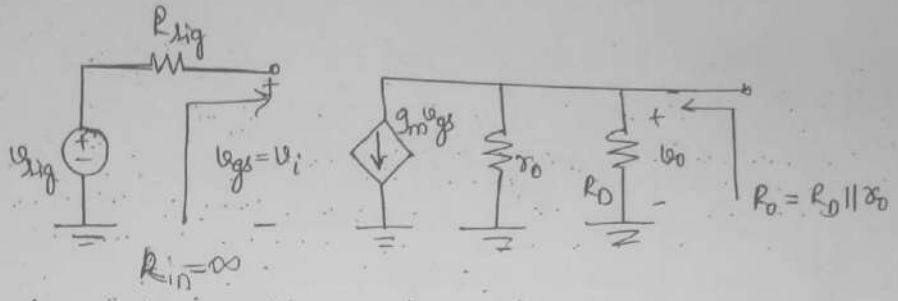
$$\therefore \boxed{G_v = \frac{R_{in}}{R_{in} + R_{sig}} \cdot A_{vo} \cdot \frac{R_L}{R_L + R_o}}$$

The common source (CS) Amplifier

CKt



The below circuit shows the amplifier with the MOSPET replaced with its hybrid-π model.



→ Let us now, find the characteristic parameters of the amplifier.

R_{in}

$$\boxed{R_{in} = \infty}$$

A_{vo}

from the circuit,

$$v_o = -(g_m v_{gs})(R_D \| r_o)$$

Since $v_{gs} = v_i$, $A_{vo} = \frac{v_o}{v_i} = -(g_m \times (R_D \| r_o))$

$$\boxed{A_{vo} \cong -g_m R_D} \quad \text{for } r_o >> R_D$$

R_o :

$$R_o = R_D \| r_o$$

for $r_o >> R_D$ $\quad \boxed{R_o \cong R_D}$

Overall vg gain G_v : To determine the overall voltage

gain G_v, we consider by considering R_L

Then $\boxed{G_v = -g_m (R_D \| R_L \| r_o)}$

A CS amplifier utilizes a MOSFET biased at $I_D = 0.25mA$ with $V_{OV} = 0.25V$ and $R_D = 20k\Omega$. The device has $V_A = 50V$. The amplifier is fed with a source having $R_{sig} = 100k\Omega$ and $R_L = 20k\Omega$. Find R_{in}, A_{vo}, R_o, A_v & G_v. To maintain reasonable linearity, the peak of the i/p sine-wave signal is limited to 10% of $(2V_{OV})$. What is the peak of the sine-wave voltage at the o/p?

R_{in} $\boxed{R_{in} = \infty}$

$A_{vo} = -g_m (R_D \| r_o)$

where $g_m = \frac{2I_D}{V_{OV}} = \frac{2 \times 0.25 \times 10^{-3}}{0.25} = 2 \times 10^{-3} \mho$

$$r_o = \frac{V_A}{I_D} = \frac{50V}{0.25mA} = 200k\Omega$$

$\therefore A_{vo} = -2 \times 10^{-3} \times (20k\Omega \| 200k\Omega)$

$\boxed{A_{vo} = -36.4}$

$R_o = R_D \| r_o = 18.2k\Omega$

$G_v = -g_m (R_D \| r_o \| R_L) = -2 \times 10^{-3} \times (18.2k \| 20k)$

$\boxed{G_v = -19}$

For linear amplification, $v_{gs} = 10\%$ of $2V_{OV}$ is chosen

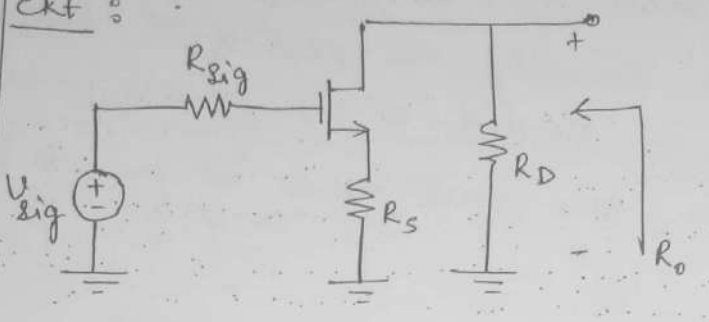
$\therefore v_{gs} = 0.1 \times 2(0.25V) = 0.05V$

$v_o = \frac{R_L}{R_L + R_o} A_{vo} \times v_i = \frac{20k}{20k + 18.2k} \times 36.4 \times 0.05 = 0.95V$

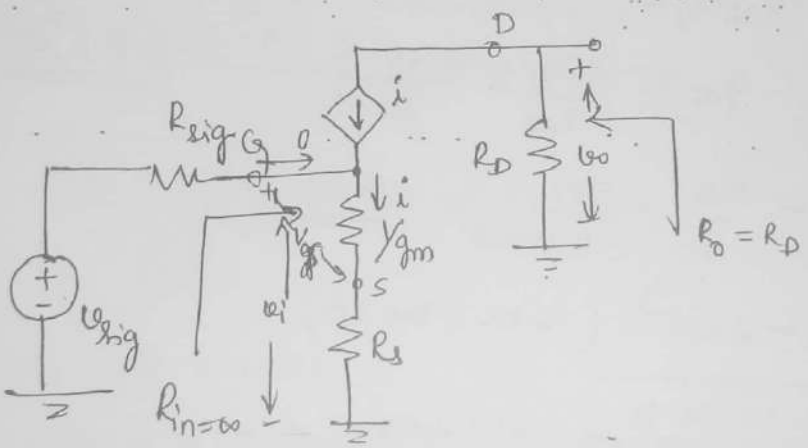
Common Source Amplifier with a Source Resistance

[NOTE: whenever a resistance is connected in the source lead, the T model is preferred. r_o is not included in the analysis. As its value is very high which has least effect in amplifier parameters But addition of r_o would unnecessarily complicate the analysis]

ckt:



Equivalent circuit with MOSFET replaced by its T-model



From the circuit,

$$-v_{gs} = v_i \times \frac{1/g_m}{1/g_m + R_S} = \frac{v_i}{1 + g_m R_S}$$

$$v_o = -i R_D$$

where $i = \frac{v_i}{1/g_m + R_S} = \left(\frac{g_m}{1 + g_m R_S}\right) v_i$

$$\therefore v_o = -\frac{g_m}{(1 + g_m R_S)} \times v_i \times R_D \Rightarrow \boxed{A_{v_o} = \frac{v_o}{v_i} = \frac{-g_m}{1 + g_m R_S} \times R_D}$$

The equation of A_{vo} indicates that including R_s reduces the voltage gain by the factor $(1+g_m R_s)$.

[NOTE: The factor $(1+g_m R_s)$ is the ~~most~~ amount of negative feedback introduced by R_s. It is also the factor by which the BW and other performance parameters improve. Because of the -ve f/b action of R_s it is known as a source-degeneration resistance]

A_v: can be obtained by simply replacing R_D by $(R_D \| R_L)$

$$\therefore A_v = \frac{-R_D \| R_L}{\frac{1}{g_m} + R_s} = \frac{-g_m (R_D \| R_L)}{1 + g_m R_s}$$

Source Follower OR Common Drain Amplifier

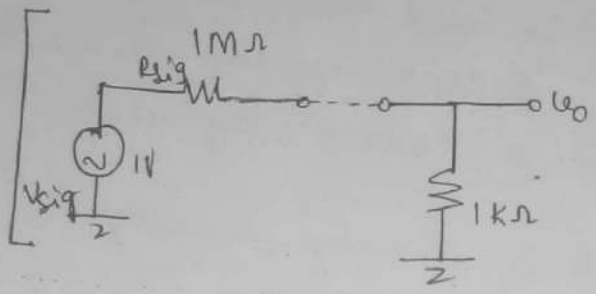
→ The voltage at the o/p terminal (source) will follow that at the i/p. Hence, the name source follower.

→ It is used as a buffer.

→ Need for voltage buffer:

Let us say, a signal source delivering a signal of reasonable-strength say 1V. with an internal resistance of 1MΩ. which suppose to be connected to a 1K-Ω

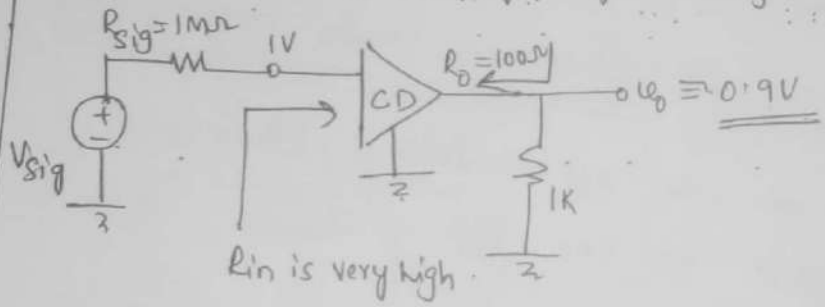
be ~~connected to a 1KΩ~~ load resistance, But connecting the source to the load directly would result in severe attenuation of the signal.



$$\Rightarrow V_o = 1V \times \frac{1K\Omega}{1.001M}$$

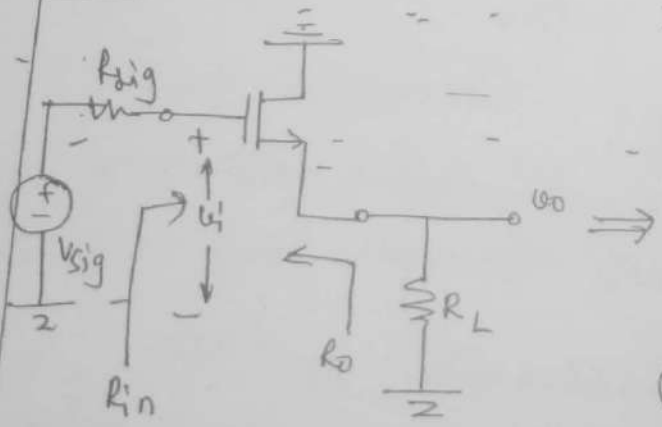
$$= 0.99V$$

Therefore, between the source and load, usually CD amplifier is connected (whose i/p resistance is very high & o/p resistance is low and voltage gain of unity). As shown below

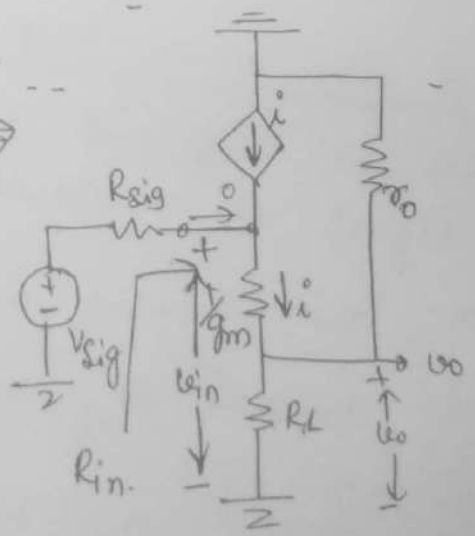


CD amplifier circuit:

CKt



Equivalent ckt by replacing transistor with T-model



characteristics parameters

R_{in} :

$$\boxed{R_{in} = \infty} \quad \text{——— (1)}$$

A_{vo} :

from the circuit,

$$v_o = v_i \times \frac{R_L}{R_L + 1/g_m}$$

$$\therefore \boxed{A_V = \frac{v_o}{v_i} = \frac{R_L}{R_L + 1/g_m}} \quad \text{——— (2)}$$

A_{vo} : (Setting $R_L = \infty$)

from (2)

$$\boxed{A_{vo} = 1} \implies \therefore v_o = v_i$$ Hence the name voltage follower.

R_o :

The o/p resistance R_o is found by setting $v_i = 0$. Now looking back into the o/p terminal, excluding R_L, R_o we see as $1/g_m$.

$$\therefore \boxed{R_o = \frac{1}{g_m}}$$

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} \times A_{vo} \times \frac{R_L}{R_L + R_o}$$

$$= \underset{(R_{in}=\infty)}{1} \times 1 \times \frac{R_L}{R_L + 1/g_m} \quad \{\text{Since } A_{vo} = 1 \text{ \& } R_{in} = \infty\}$$

$$\boxed{G_v = \frac{R_L}{R_L + 1/g_m}}$$

$\therefore$ G_v will be lower than unity

Summary and comparison

CS Amplifier:

* Most widely used amplifier ~~used~~ as voltage amplifier
* The circuit provides very high Z_{in} and medium Z_o
* Both voltage and current gain are medium.
* o/p is the inverse of the i/p

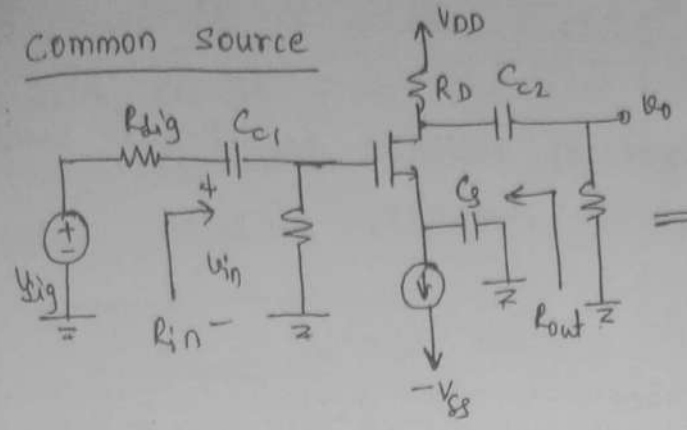
Common Gate amplifier:

* Provides a low i/p impedance and offers very high o/p impedance. Because of its low i/p resistance, the CG amplifier alone has very limited application.
* CG amplifier has excellent high-frequency response. Hence, usually CG amplifier can be combined with CS amplifier, ~~So that~~ high Z_{in} of CS amplifier and high frequency response of CG amplifier can be availed.
* provides high voltage gain but poor current gain
* i/p & o/p are in phase.

common drain Amplifier:

* Popularly known as source follower
* Offers very high Z_i & very low Z_o. This feature ~~enables us~~ to use as buffer.
* The voltage gain is unity but very high current gain.
* I/p and o/p signals are in phase.
* Characteristics of MOS amplifiers is as ~~shown~~ given in next page

1 Common Source



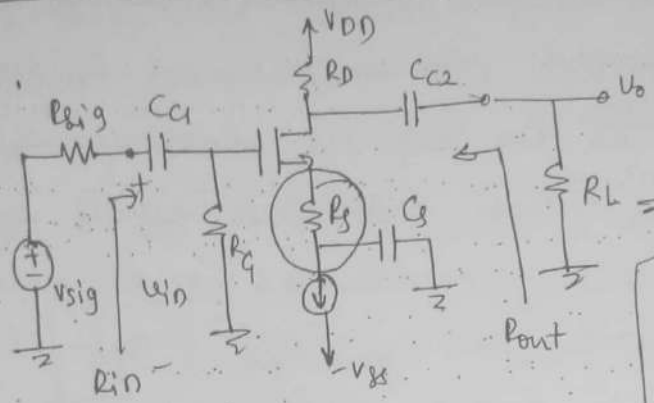
$R_{in} = R_G$

$A_v = -g_m(r_o \| R_D \| R_L)$

$R_{out} = r_o \| R_D$

$G_V = \dfrac{-R_G}{R_G + R_{sig}} g_m (r_o \| R_D \| R_L)$

2 Common Source with. Rs



Neglecting r_o

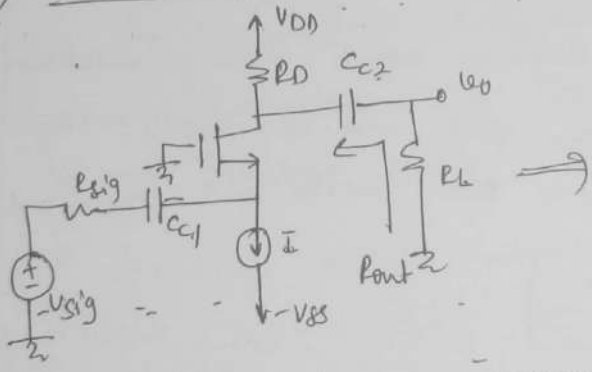
$R_{in} = R_G$

$A_v = \dfrac{R_D \| R_L}{\frac{1}{g_m} + R_s} = \dfrac{g_m(R_D \| R_L)}{1 + g_m R_s}$

$R_{out} = R_D$

$G_V = \dfrac{-R_G}{R_G + R_{sig}} \cdot \dfrac{g_m(R_D \| R_L)}{1 + g_m R_s}$

3) Common gate



Neglecting r_o

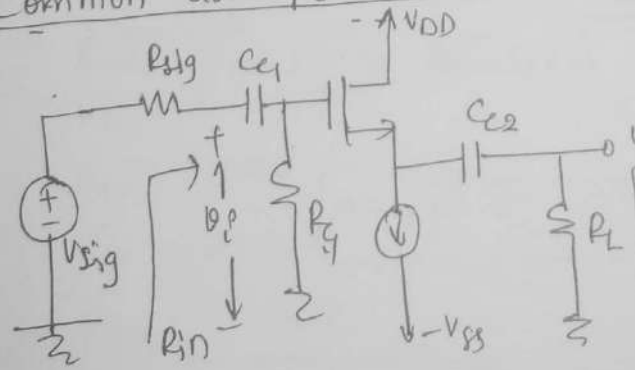
$R_{in} = 1/g_m$

$A_v = g_m(R_D \| R_L)$

$R_{out} = R_D$

$G_V = \dfrac{1}{1 + g_m R_{sig}} \cdot g_m(R_D \| R_L)$

4 Common drain / source follower:



$R_{in} = R_G$

$A_v = \dfrac{r_o \| R_L}{(r_o \| R_L) + 1/g_m}$

$R_{out} = r_o \| 1/g_m \cong 1/g_m$

$G_v = \dfrac{R_G}{R_G + R_{sig}} \cdot \dfrac{r_o \| R_L}{(r_o \| R_L) + 1/g_m}$

MOSFET Internal capacitances :

There are two types of built-in capacitances called Internal capacitances in MOSFET

① gate capacitance

② Junction capacitance

Gate capacitance : The gate (Polysilicon) forms a parallel-plate capacitor with the channel. Here, oxide layer serve as the capacitor dielectric which is denoted as C_{ox}. These capacitances effects can be modeled by including capacitances in the model between its 4 terminals as C_{gs}, C_{gd} & C_{gb} (bulk). Its effects are different in 3 different regions

a) **In linear region :**

* channel will be of uniform depth. The gate-channel capacitance will be WLC_{ox} and can be modeled by dividing it equally between the source and drain ends

$$\boxed{C_{gs} = C_{gd} = \frac{1}{2} WLC_{ox}}$$

b) **In saturation region :**

* Channel depth is maximum at source end zero at drain end

$$\therefore \boxed{C_{gs} = \frac{2}{3} WLC_{ox} \;\&\; C_{gd} = 0}$$

c) **Cut-off region :**

* No channel exists $\therefore \boxed{\begin{array}{l} C_{gs} = C_{gd} = 0 \\ C_{gb} = WLC_{ox} \end{array}}$

(d) There is an additional small capacitive component which results from the fact that the source and drain diffusions extend slightly under the gate oxide which is known as overlap capacitance (C_{ov}).

$$C_{ov} = W L_{ov} C_{ox}$$. Typically $L_{ov} = (0.05 \text{ to } 0.1) \times L$.

(e) Junction capacitances : There exists 2-junctions in the device - one between the drain-substrate and other between source-substrate. ~~They are modeled as~~ The capacitance of these junctions are modeled as C_{db} & C_{sb} respectively.

$$C_{db} = \frac{C_{dbo}}{\sqrt{1 + \frac{V_{DB}}{V_0}}} \quad \& \quad C_{sb} = \frac{C_{sbo}}{\sqrt{1 + \frac{V_{SB}}{V_0}}}$$

$C_{dbo} \rightarrow$ capacitance at $V_{SB} = 0$

$C_{sbo} \rightarrow$ capacitance at $V_{SB} = 0$

$V_0 \rightarrow$ Junction built-in potential. (0.6 – 0.8V).

For n-channel MOSFET, with $t_{ox} = 10nm$, $L = 1.0\mu m$, $W = 10\mu m$, $L_{ov} = 0.05\mu m$, $C_{sbo} = C_{dbo} = 10fF$, $V_0 = 0.6V$ $V_{SB} = 1V$ & $V_{DS} = 2V$. calculate C_{ox}, C_{ov}, C_{gs}, C_{gd}, C_{sb} & C_{db} when transistor operating in saturation region.

Ans

$C_{ox} = 3.45 fF/\mu m^2$ $\quad C_{sb} = 6.1 fF$

$C_{ov} = 1.72 fF$ $\quad C_{db} = 4.1 fF$

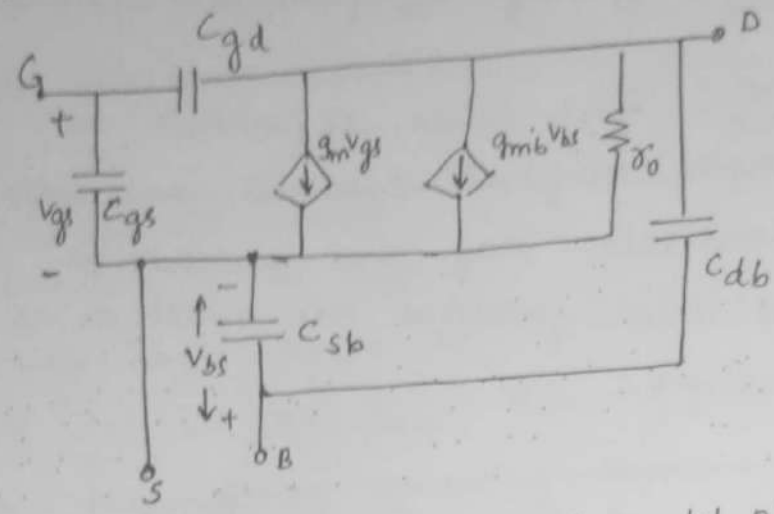
$C_{gs} = 24.7 fF$

$C_{gd} = 1.72 fF$

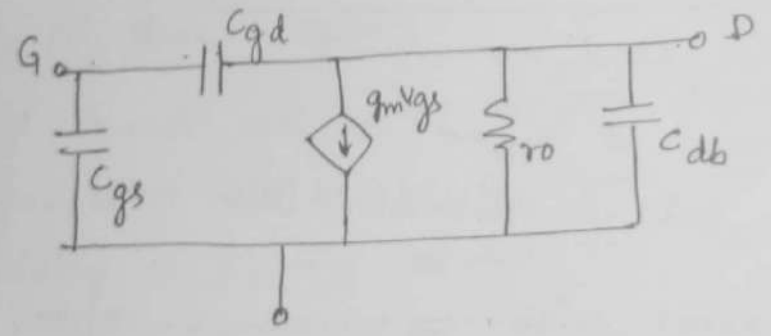
$$\left\{ C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 3.9 \times 8.854 \times 10^{-12} \text{ F/m} \right.$$

High frequency MOSFET model :

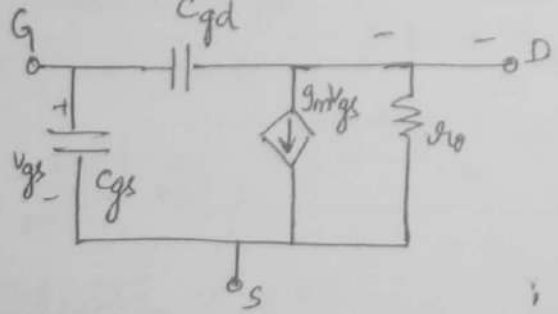
→ A small signal model of the MOSFET, including the 4 capacitances C_{gs}, C_{gd}, C_{sb} & C_{db} is as shown below



Following is the small signal model of MOSFET ; when source and bulk are at same voltage

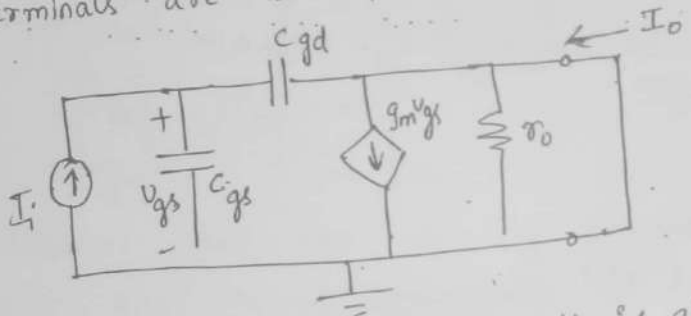


usually C_{db} can be neglected as its effect is insignificant and resulting in significant simplification of manual analysis. The below is the model with neglecting C_{db} -



The MOSFET unity gain frequency

* This is the figure of merit for the high frequency operation of the MOSFET.
* which is also known as transition frequency (f_T)
* It can be defined as "The frequency at which the short circuit current-gain of the common source configuration becomes unity."
* Let us consider the MOSFET hybrid-π model of CS amp. To find the short circuit current gain; the i/p is fed with a current-source signal I_i and the o/p terminals are shorted.



The current in the short circuit is given by

$$I_o = g_m V_{gs} - sC_{gd} V_{gs} \quad \text{---(1)}$$

As C_{gd} is very small, the second term can be ignored. Then -

$$I_o \simeq g_m V_{gs} \quad \text{---(2)}$$

from the model, V_{gs} can be expressed in terms of I_i as

$$V_{gs} = I_i / s(C_{gs} + C_{gd})$$

∴ Short ckt current gain is

$$\frac{I_o}{I_i} = \frac{g_m}{sC(C_{gs} + C_{gd})} \quad \text{---(3)}$$

→ For physical frequencies, $s = j\omega$, it can be seen that the magnitude of the current gain becomes unity at the frequency

$$\omega_T = g_m / (C_{gs} + C_{gd})$$

Thus, the unity-gain frequency

$$f_T = \omega_T / 2\pi$$

$$\boxed{f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}}$$

→ higher the f_T, more effective the device is.

[NOTE: In problems As internal capacitances are different for each region, in problems, identify in which region the transistor is operating and calculate capacitances.]

cut-off	Linear	sat^n
$C_{gs} = C_{gd} = 0$	$C_{gs} = C_{gd} = \frac{1}{2} WLC_{ox}$	$C_{gs} = \frac{2}{3} WLC_{ox}$
$C_{gb} = WLC_{ox}$	$C_{gb} = 0$	$C_{gd} = 0$
		$C_{gb} = 0$

Calculate f_T for the n-channel MOSFET whose capacitances are $C_{ox} = 3.45\ fF/\mu m^2$; $C_{ov} = 1.72\ fF$, $C_{gs} = 24.7\ fF$; $C_{gd} = 1.72\ fF$; $C_{sb} = 6.1\ fF$ & $C_{db} = 4\ fF$. Assume operation at $100\mu A$ & $K_n' = 160\ \mu A/V^2$. $W = 10\ \mu m$, $L = 1.0\ \mu m$

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}$$

$$g_m = \sqrt{K_n' \frac{W}{L}} \times \sqrt{2 I_D}$$

$$= \sqrt{160\ \mu A/V^2} \times \sqrt{\frac{10}{1}} \times \sqrt{2 \times 100\mu A}$$

$$= 0.0126 \times 3.162 \times 0.0141 = 0.56 \times 10^{-3}$$

$$f_T = \frac{0.56 \times 10^{-3}}{2 \times \pi \times (24.7\ fF + 1.72\ fF)} = 3.37\ GHz$$

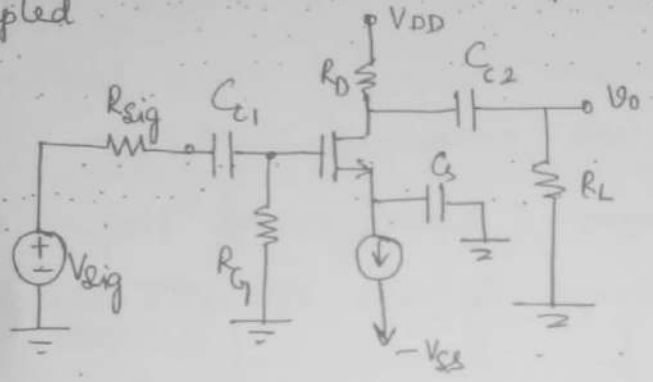
Frequency Response of the CS Amplifier

→ gain of the CS amplifier depends on the frequency of the applied i/p signal.

→ 3 frequency bands.

① Low frequency band
② Mid frequency band
③ upper frequency (High) band.

→ Let us consider the CS amplifier with capacitively coupled



→ Assume that the coupling capacitors C_{C1} and C_{C2} and the bypass capacitor C_S are acting as perfect short circuits at all signal frequencies of interest. Also internal capacitances are neglected. This situation applies over a wide band of frequencies called as MIDBAND. In Midband frequencies gain is maximum and constant.

ie, $$\bar{A}_M = \frac{\bar{V}_o}{V_{sig}} = -\frac{R_G}{R_G + R_{sig}} A_{vo} (r_o \| R_D \| R_L)$$

→ The frequencies below and above to Midband frequencies are called Lower & High frequency band at which gain falls off.

→ Reason for gain Roll-off

* The gain fall off in the low-frequency band is due to the fact that, as the signal frequency is reduced, impedances of C_{C1}, C_{C2} & C_S increases and they no longer behave as short circuits. They reduce the voltage gain. $X_C = \frac{1}{2\pi f C}$

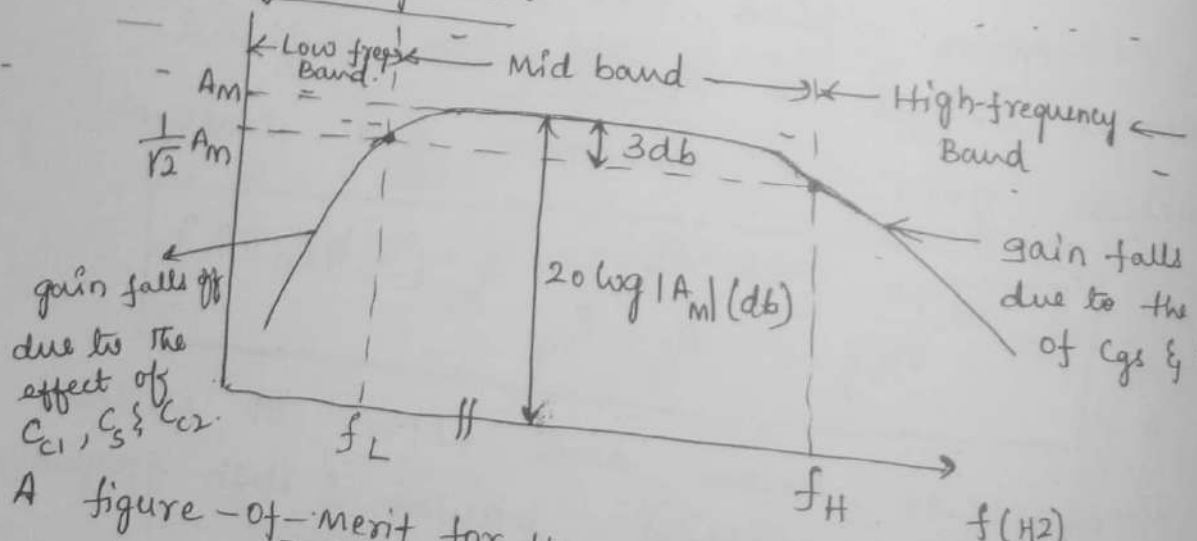
* The gain falls off in the high-frequency band as result of C_{gs} and C_{gd}, Even though, their value is small, their impedances at high frequencies decrease and thus they no longer be considered as open circuits.

→ Mid band is useful frequency band.

→ f_L & f_H are Lower & upper cut-off frequencies at which gain drops by 3db below its value at midband.

→ Amplifier $\boxed{B.W = f_H - f_L}$. Since usually $f_L << f_H$ $\boxed{B.W \cong f_H}$

Frequency Response:

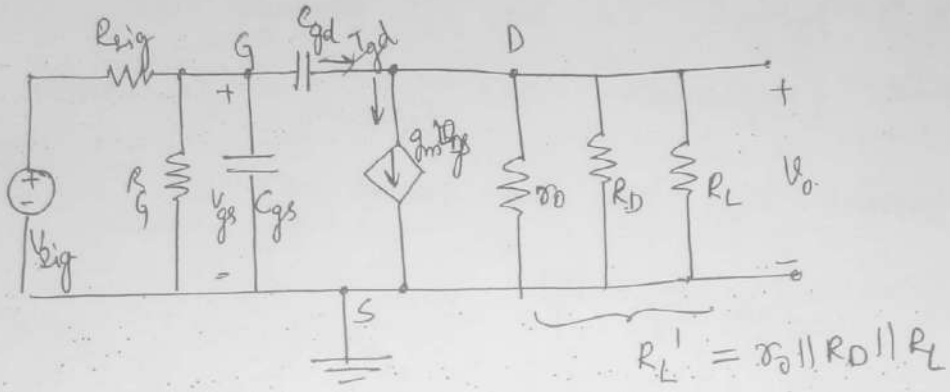


→ A figure-of-merit for the amplifier is its gain-bandwidth product.

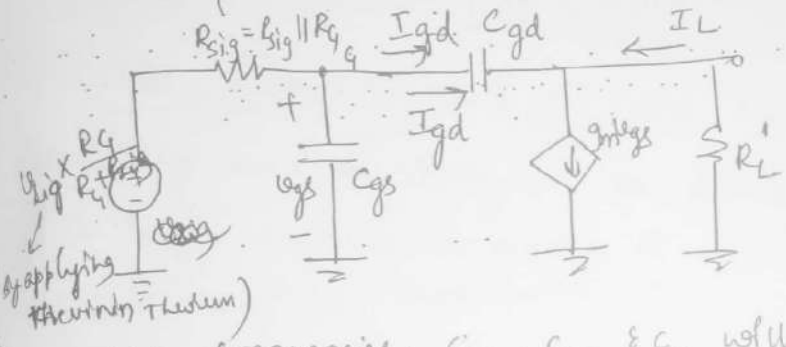
$\boxed{GB = |A_m| \times BW}$

High frequency Response :

→ To determine the gain, Transfer function of the amplifier at high frequencies, let us draw the high frequency model of common source amplifier.



→ simplified circuit of above circuit.



→ At high frequencies, C_{C1}, C_{C2} & C_S will behaving as perfect ~~switch~~ short circuit. Hence they do not appear in high frequency model.

→ C_{gd} is the capacitance which connects the o/p node to the i/p side.

→ From the circuit,

$$I_L = (g_m v_{gs} - I_{gd})$$

where $g_m v_{gs}$ is the o/p current of the transistor, and I_{gd} is the current supplied through the very small capacitance C_{gd} which is very small & can be neglected.

$\therefore I_L = g_m v_{gs}$

$\therefore v_0 = -I_L \times R_L' = -g_m v_{gs} \times R_L'$

where $R_L' = r_0 \| R_D \| R_L$

Hence $v_0 = -g_m v_{gs} R_L'$ is the o/p voltage at mid band frequencies.

→ The current I_{gd} can be found as.

$$I_{gd} = s C_{gd} (v_{gs} - v_0)$$

$$= s C_{gd} [v_{gs} - (-g_m R_L' v_{gs})]$$

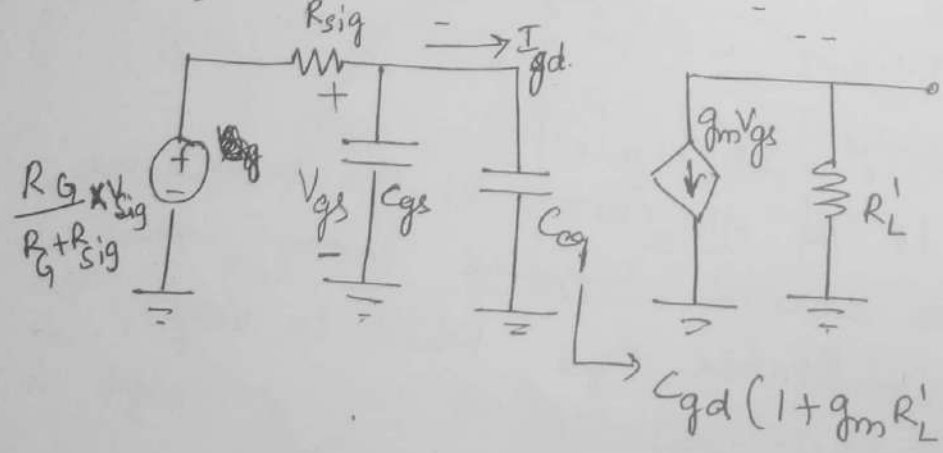
$$\boxed{I_{gd} = s C_{gd} (1 + g_m R_L') v_{gs}} \rightarrow \text{current due to } C_{gd}$$

As C_{gd} is connected b/n i/p & o/p terminals, its equivalent capacitance at i/p side can be shown as C_{eq} as long as it draws a current equal to I_{gd}.

$\therefore s C_{eq} v_{gs} = s C_{gd} (1 + g_m R_L') v_{gs}$

$$\therefore \boxed{C_{eq} = C_{gd} (1 + g_m R_L')} \rightarrow \text{Miller capacitance i/p.}$$

Including C_{eq}, the above circuit can be redrawn as -



we see the above circuit as a single-time-constant circuit of lowpass type. Then V_{gs} is

$$V_{gs} = \left(\frac{R_G}{R_G + R_{sig}} V_{sig}\right) \cdot \frac{1}{1 + \frac{s}{\omega_0}}$$

where $\omega_0 = \frac{1}{C_{in} R'_{sig}}$

where $C_{in} = C_{gs} + C_{eq}$

$$\therefore \frac{V_o}{V_{sig}} = \frac{-g_m R'_L V_{gs}}{V_{gs}\left(\frac{R_G + R_{sig}}{R_G}\right)\left(1 + \frac{s}{\omega_0}\right)}$$

$$\frac{V_o}{V_{sig}} = \left(\frac{R_G}{R_G + R_{sig}}\right)(g_m R'_L) \times \frac{1}{1 + \frac{s}{\omega_0}}$$

which can be represented as

$$\frac{V_o}{V_{sig}} = \frac{A_m}{1 + s/\omega_H}$$

where $\omega_H = \frac{1}{C_{in} R'_{sig}}$

$$\boxed{f_H = \frac{\omega_H}{2\pi} = \frac{1}{2\pi C_{in} R'_{sig}}}$$

Reference

$$V_{gs} = \frac{\frac{R_G}{R_G + R_{sig}} V_{sig} \times \frac{1}{sC_{in}}}{\frac{1}{sC_{in}} + R_{sig}}$$

where $(C_{in} = C_{gs} + C_{eq})$

$$V_{gs} = \frac{\frac{R_G}{R_G + R_{sig}} \times V_{sig}}{1 + sC_{in} R'_{sig}}$$

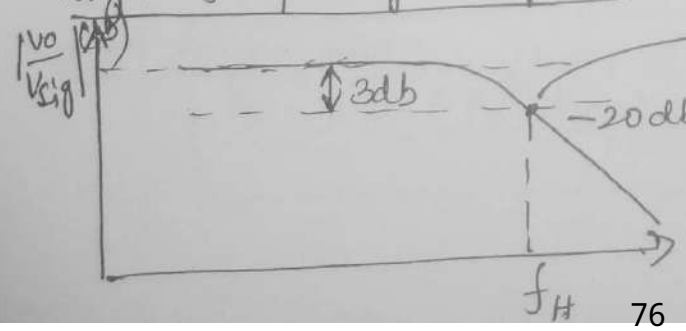
$$= \frac{R_G}{R_G + R_{sig}} V_{sig} \times \frac{1}{1 + \frac{s}{\omega_0}}$$

$\because RC = t$

$\frac{1}{RC} = \omega$

ie, $\omega_0 = \frac{1}{R'_{sig} C_{in}}$

→ High frequency Response



#① Find the mid-band gain A_M and the upper 3-db frequency f_H of a CS amplifier fed with a signal source having an internal resistance $R_{sig} = 100\,k\Omega$. The amplifier has $R_G = 4.7\,M\Omega$, $R_D = R_L = 15\,K\Omega$, $g_m = 1\,mA/V$, $r_o = 150\,K\Omega$, $C_{gs} = 1\,PF$ and $C_{gd} = 0.4\,PF$

Soln $$A_M = -\frac{R_G}{R_G + R_{sig}} g_m R_L'$$

$R_L' = r_o \| R_D \| R_L = 7.14\,k\Omega$; $g_m R_L' = 1 \times 7.14 = \underline{7.14\,V/V}$

$$A_M = -\frac{4.7}{4.7+0.1} \times 7.14 = -7\,V/V$$

$C_{eq} = (1 + g_m R_L') C_{gd} = \underline{3.26\,PF}$

$C_{in} = C_{gs} + C_{eq} = \underline{4.26\,PF}$

Then the upper 3-db frequency f_H is

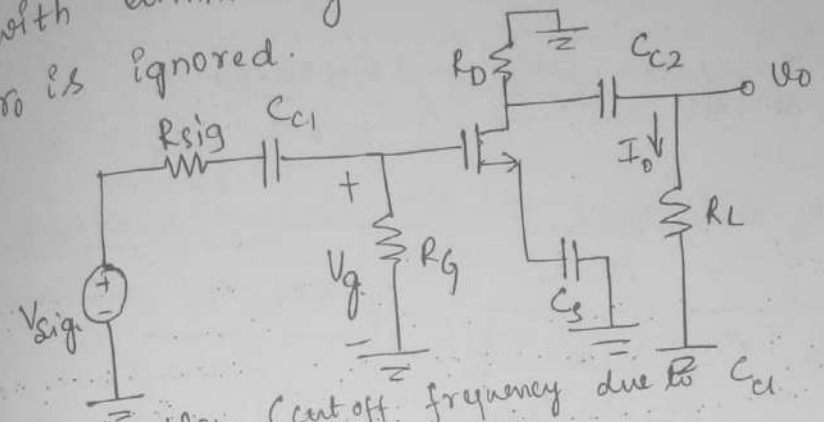
$$f_H = \frac{1}{2\pi C_{in}(R_{sig} \| R_G)} = \underline{382\,KHz}$$

#② For the above problem, find the values of A_M and f_H that result when the signal source resistance is reduced to $10\,K\Omega$. (Ans: $A_V = -7.12$, $f_{it} = \underline{3.7\,MHz}$)

If it is possible to replace the MOSFET used in the above problem (#) with another having the same C_{gs} but smaller C_{gd}, what is the maximum value that its C_{gd} can be in order to obtain an f_H of at least $1\,MHz$ (Ans: 0.08 PF)

The low frequency Response.

Let us consider the CS amplifier to determine its low-frequency transfer function with eliminating dc sources. The effect of r_o is ignored.



To find ω_{p1} (cut off frequency due to C_{C1}) from the ckt,

$$V_g = V_{sig} \frac{R_G}{R_G + \frac{1}{sC_{C1}} + R_{sig}} = V_{sig} \frac{R_G}{(R_G + R_{sig}) + \frac{1}{sC_{C1}}}$$

which can be written in the an alternate form as

$$V_g = V_{sig} \frac{R_G sC_{C1}}{(R_G + R_{sig})sC_{C1} + 1}$$

$$= V_{sig} \times \frac{R_G \cancel{sC_{C1}}}{(R_G + R_{sig})\cancel{sC_{C1}}\left[1 + \frac{1}{(R_G + R_{sig})sC_{C1}}\right]}$$

$$V_g = V_{sig} \times \frac{R_G}{(R_G + R_{sig})} \frac{s}{s + \frac{1}{C_{C1}(R_G + R_{sig})}} \quad \text{---(A·B1)}$$

Here, $\boxed{\omega_0 = \frac{1}{C_{C1}(R_G + R_{sig})} = \omega_{p1}}$

To find ω_{p2} : we determine I_d

$$I_d = \frac{V_g}{\frac{1}{g_m} + \frac{1}{sC_s}} = g_m V_g \times \frac{s}{s + \frac{g_m}{C_s}}$$

Here, $\boxed{\omega_{p2} = \frac{g_m}{C_s}}$

To find ω_{p3} :

From the circuit, $I_o = -I_d \frac{R_D}{R_D + \frac{1}{sC_{C2}} + R_L}$

$$V_o = I_o R_L = -I_d \frac{R_D R_L}{R_D + R_L} \cdot \frac{s}{s + \frac{1}{C_{C2}(R_D + R_L)}}$$ → similar to I case.

Here, $\boxed{\omega_{p3} = \frac{1}{C_{C2}(R_D + R_L)}}$

Then, the overall low frequency transfer function can be given by

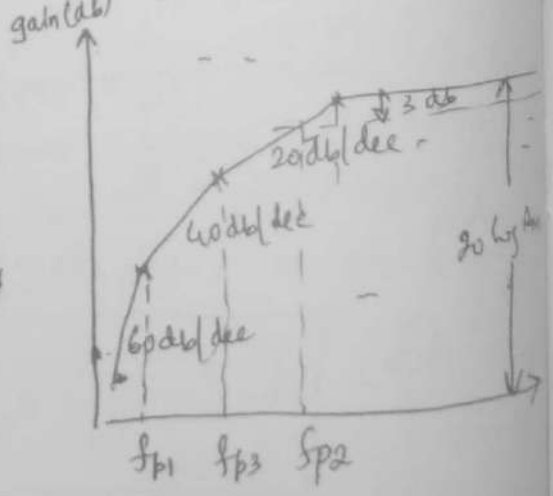
$$\boxed{\frac{V_o}{V_{sig}} = -\left(\frac{R_G}{R_G + R_{sig}}\right)\left[g_m(R_D \parallel R_L)\left(\frac{s}{s+\omega_{p1}}\right)\left(\frac{s}{s+\omega_{p2}}\right)\left(\frac{s}{s+\omega_{p3}}\right)\right]}$$

where $\omega_{p1}, \omega_{p2}, \omega_{p3}$ are called break frequencies.

→ one of the 3 break frequencies can be much higher than others. In such cases it is the highest frequency break point that will determine the lower 3-db frequency. ω_{p2} is usually higher than ω_{p1} & ω_{p3}.

∴ $\boxed{f_L = f_{p2}}$

Low frequency Response



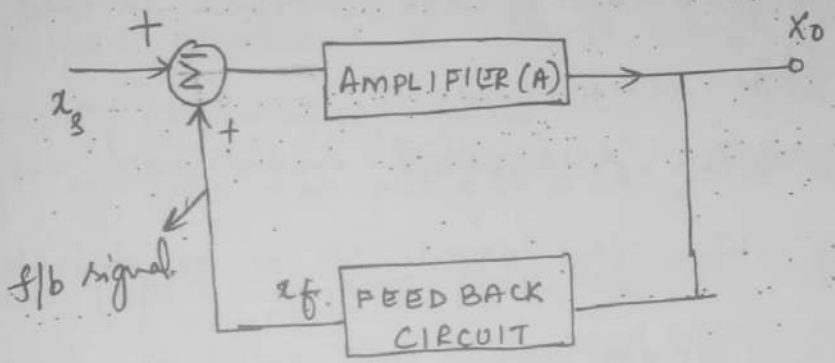
* ——— end ——— * ———

OSCILLATORS

→ Oscillators are the electronic circuits which produces a periodic, oscillating electronic signal by themselves. i.e, without applying any ac i/p signal.

→ Types of waveforms that can be produced
* square, sinusoidal, triangular or pulse.

→ Basic structure of any oscillator.



→ Oscillator circuit consists of an amplifier and feedback circuit. Broth introduces a phase shift of 180°.

→ In the process of feedback, a part of o/p is sampled and fed back to the input of the amplifier. These two signals are with same phase. Hence and the type of feedback is POSITIVE

NOTE: In an actual oscillator circuit, no i/f signal will be present.

→ The +ve feed back results into oscillations. Hence this type of f/b is employed in oscillators.

The oscillation Criterion

BARKHUASEN CRITERIA :

→ To obtain sustained oscillations, following Barkhausen conditions must be satisfied as below.

① $|A\beta| = 1$

where $A \rightarrow$ gain of the amplifier

$\beta \rightarrow$ Feed back factor.

② Total phase shift of the circuit should be 0° or 360°.

Hence, to provide sustained sinusoidal oscillations of frequency ω_0, the condition to be satisfied is,

$$A(j\omega_0) \cdot \beta(j\omega_0) = 1$$

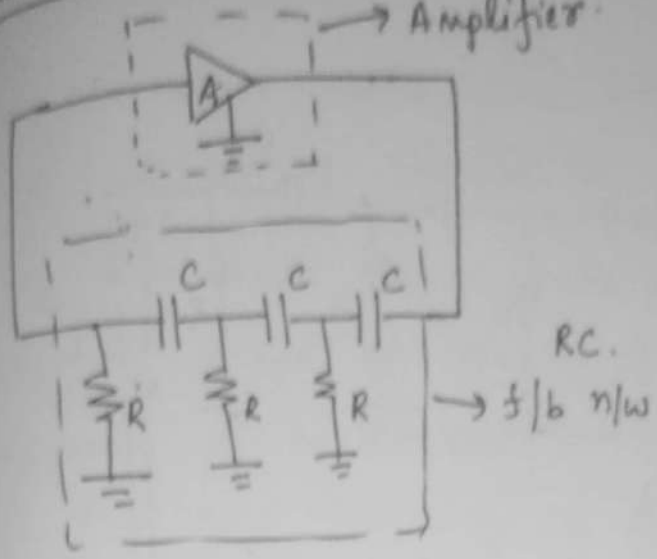
That is, at ω_0, the phase of the loop gain should be zero and the magnitude of the loop gain should be unity. This is known as the BARKHAUSEN CRITERION.

RC- phase shift oscillator :

→ Basic concept : RC phase shift oscillator basically consist of amplifier and a f/b network consisting of resistors and capacitors arranged in ladder fashion.

→ The circuit will oscillate at the frequency for which the phase shift of the RC network is 180°.

General structure



→ Amplifier produces 180° phase shift. Each RC segment produces 60° phase shift. Thus total phase shift of (180° + 60° + 60° + 60° = 360°) 360° is obtained.

→ When $|A\beta| = 1$ & loop phase shift of 360° is maintained circuit produces the oscillations with the frequency of

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

→ The required β value should be $\frac{1}{29}$.

→ ∴ For the loop gain $|A\beta|$ to be greater than unity, the gain of the amplifier must be greater than $\frac{1}{\beta}$ or 29.

FET - Based phase - shift oscillator :

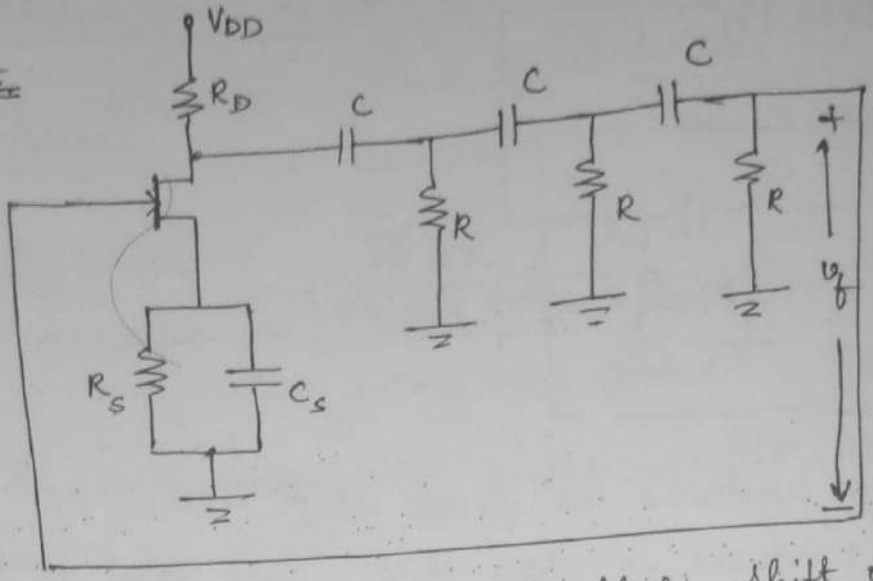
→ The circuit consist of self biased amplifier with the gain A ~~and~~ a f/b n/w with R & C components.

$$A = g_m R_D'$$

where $R_D' = \frac{R_D r_d}{R_D + r_d}$

→ The feedback network consists of three cascaded RC sections.

Ckt



→ FET amplifier provides a phase shift of 180°, The remaining 180° phase shift will be provided by the feedback network to obtain a total phase shift of 360° around the loop

→ Each RC section is designed so as to provide a phase shift of 60° at the desired frequency of oscillation.

→ In practice, the sections do not provide a phase shift of exactly 60°; due to the loading of RC section on O/P impedance of the FET amplifier

-- By designi selecting $R >> R_D^{-1}$ ($R_D' = r_d \| R_D$) the feedback n/w does not load the amplifier.

→ The frequency of oscillations depend on R & C

$$f = \frac{1}{2\pi\sqrt{6}RC}$$

→ For the sustained oscillations, $|A| > g_m R_D'$ & $g_m R_D' > 29$

$\Rightarrow |A| > 29$ & $\beta = \frac{1}{29}$

LC oscillators:

LC oscillators uses BJT/FET amplifier and LC tuned circuit or crystal as f/b CKt.

→ They are used to generate oscillations in the frequency range of 100 KHz to Mega Hertz.

→ Frequency of oscillations will be determined by the resonance frequency of parallel LC tuned ckt.

→ LC tuned circuit is also known as tank circuit.

→ They exhibit higher Q (quality factor) than RC type.

[Q → It is a measure of how underdamped an oscillator or resonator is]

→ However, LC oscillators are difficult to tune over wide ranges.

→ Two commonly used LC-tuned oscillators are Colpitts & Hartley oscillator.

Colpitts oscillators:

→ which uses two capacitors and one inductor in feedback network & produces phase shift of 180°.

→ The amplifier stage uses divice like transistor, or OPAMP. which produces 180° phase shift

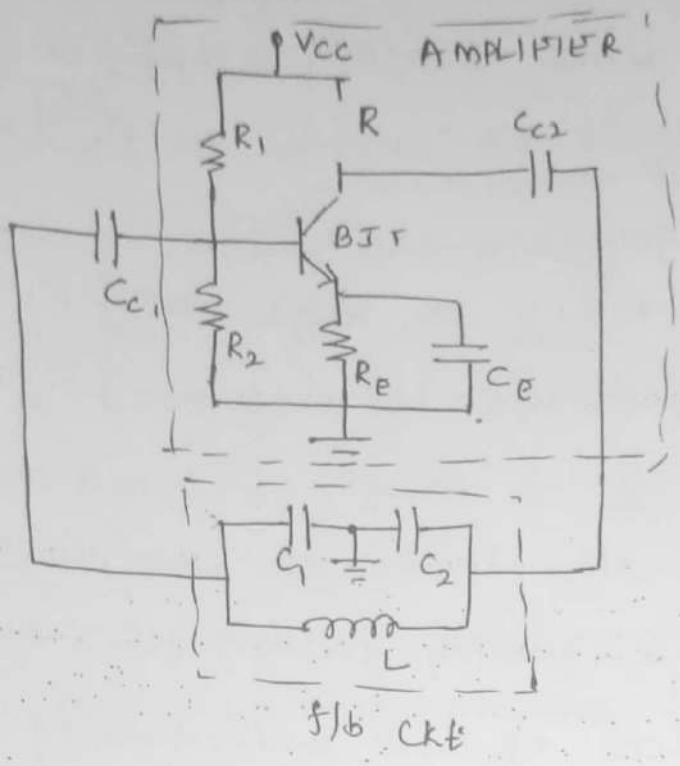
→ Total phase shift produced will be 180°+180° = 360°.

→ The basic structure is as shown in next page.

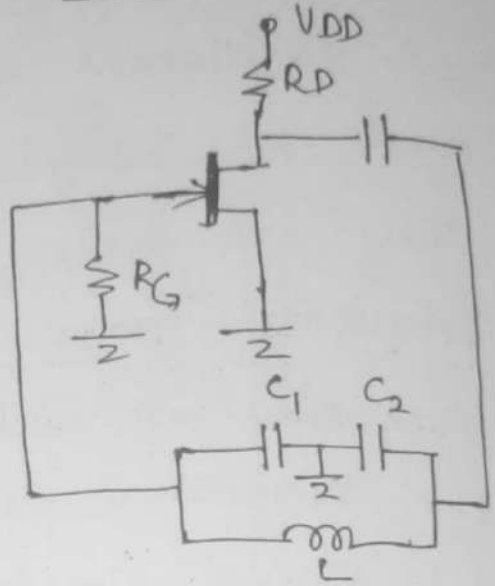
→ Frequency of oscillation is determined by

$$f_0 = \frac{1}{2\pi\sqrt{L \times C_{eq}}} \quad \text{where } C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$$

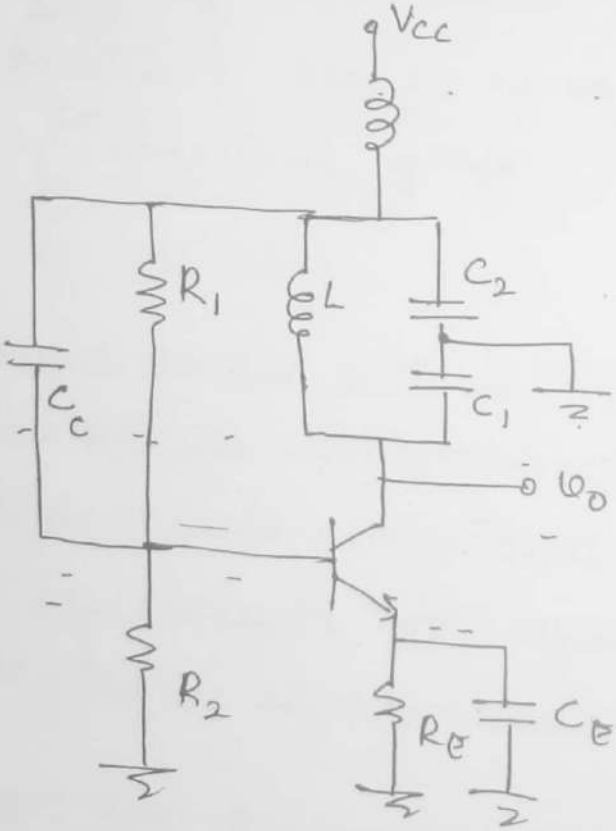
BJT version



FET version



Alternatively the above circuit can also be written as below (given in text book)



Drawback of colpitts oscillator

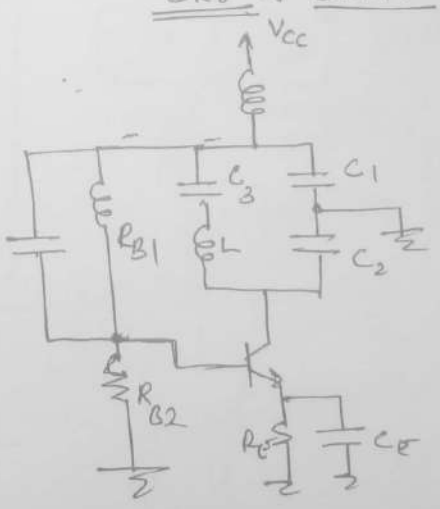
Frequency stability is very poor. Because f depends on the capacitances C_1 & C_2. As these two capacitances are shunted by the stray capacitances of the transistor, the o/p frequency is not same as the designed value and also not stable.

How to overcome the problem ?: CLAP OSCILLATOR

→ To overcome the above said problem, the inductor L is replaced by a series combination of L & C_3. It is required to take small value for C_3 compared to C_1 & C_2. As $C_3 << C_1, C_2$, the frequency of oscillation depends only on C_3. Hence, improves the stability. In this circuit frequency of oscillation becomes independent of C_1, C_2 and stray capacitance. It depends only on L & C_3.

→ Such modified colpitts oscillator is known as clapp oscillator.

CKt of CLAPP OSCILLATOR



→ $\omega_0 = \frac{1}{\sqrt{LC}}$

where $\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$

But, as $C_3 << C_1, C_2$,

$C \simeq C_3$

$\therefore \omega_0 = \frac{1}{\sqrt{LC_3}}$

Hartley oscillator :

→ Hartley oscillator uses two inductive reactances and one capacitive reactance in its f/b n/w.

→ The amplifier stage uses an active device like transistor in CE/CS configuration. Hence produces 180° phase shift. Resistors R_1 & R_2 are the biasing resistors. The RFC is the Radio frequency choke. which acts as open for ac, & short for dc.

→ As the reactance is zero and causes no problem for dc conditions.

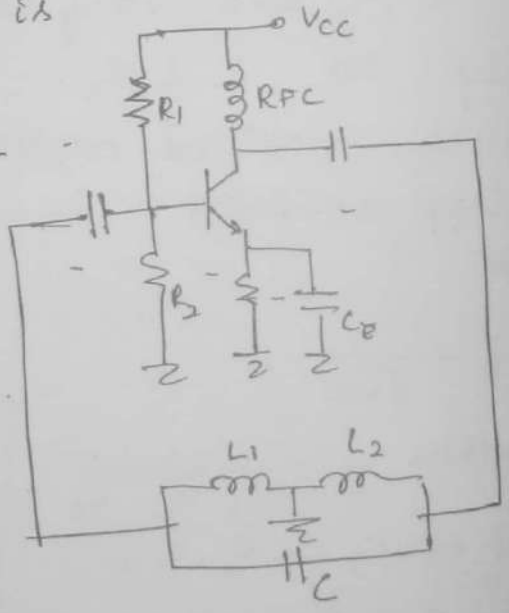
→ working of tank circuit: As the centre of L_1 & L_2 is grounded, when upper end becomes positive, the lower becomes negative, and vice versa. so the LC f/b network gives an additional phase shift of 180°. Thus the overall phase shift of the circuit becomes 360°,

→ Frequency of oscillation is given by

$$f = \frac{1}{2\pi\sqrt{C L_{eq}}}$$

where $L_{eq} = L_1 + L_2$

ckt



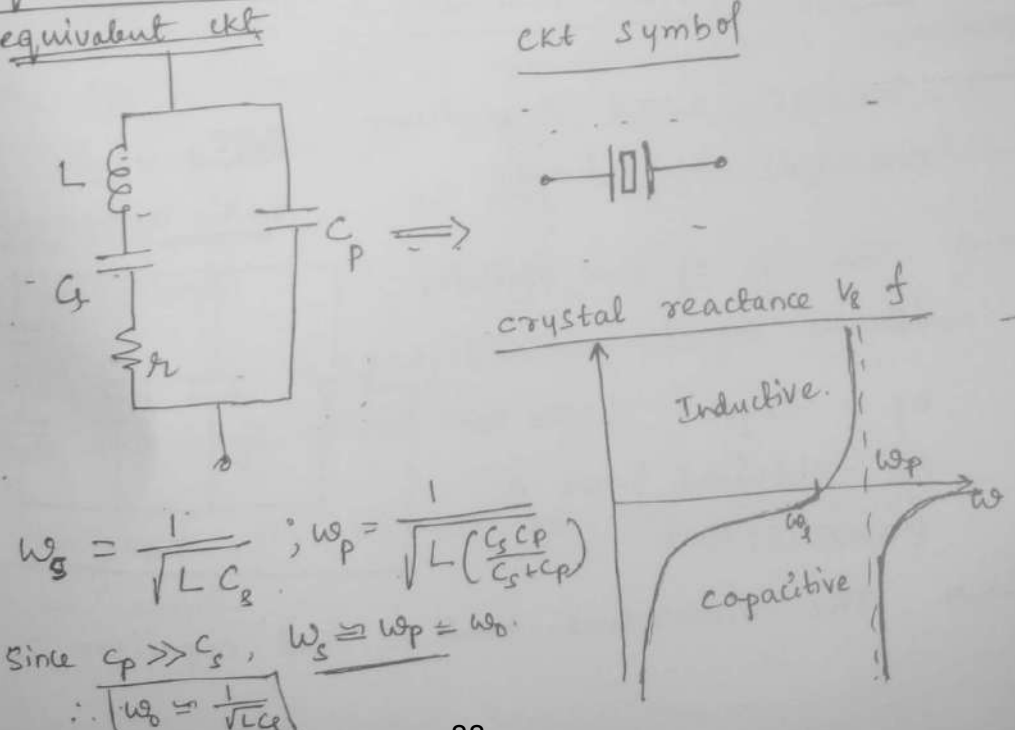
CRYSTAL OSCILLATORS

They uses piezoelectric crystal as a resonant circuit. The crystal has a greater stability in holding constant frequency. Hence, are used in transmitters and recievers.

→ Crystal oscillator works with the piezoelectric property of the crystal.

→ Piezo electric property: when a mechanical stress is applied across one of its faces, a difference of potential develops across the opposite faces. This property of the crystal is called the piezoelectric effect. Similarly, a voltage applied across one set of faces of the crystal causes mechanical vibrations. These vibrations have natural resonent frequency dependent on the crystal.

→ Equivalent circuit of the crystal:



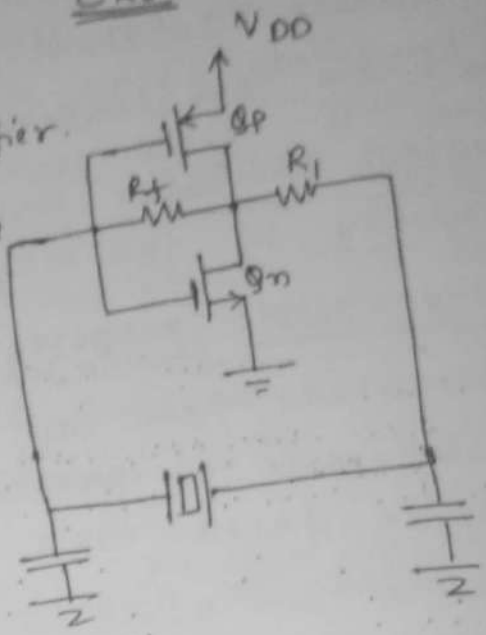
$$\omega_s = \frac{1}{\sqrt{L C_s}} \quad ; \quad \omega_p = \frac{1}{\sqrt{L\left(\frac{C_s C_p}{C_s + C_p}\right)}}$$

Since $C_p \gg C_s$, $\omega_s \simeq \omega_p \simeq \omega_0$.

$$\therefore \boxed{\omega_0 \simeq \frac{1}{\sqrt{LC_s}}}$$

A pierce crystal oscillator using cmos inverter as an amplifier

CKt



→ The circuit utilizes a cmos inverter as amplifier.

→ The resistor R_f determines a dc operating point in the high gain region of the cmos inverter.

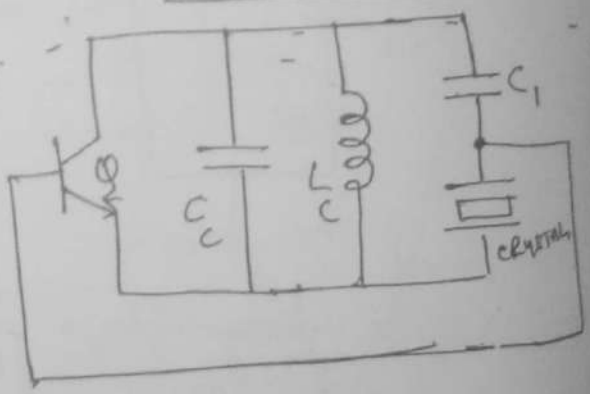
→ The resistor R_1 together with capacitor C_1 provides a low pass filter that do not allow the circuit from oscillating at a higher harmonic of the crystal frequency.

→ This is extreamely stable oscillator.

Miller crystal oscillator

→ Generally used in electronechanical applications.

Basic Miller topology



→ The I/P of this oscillator is a signal generated by a crystal & the O/P is obtained from a tank circuit.

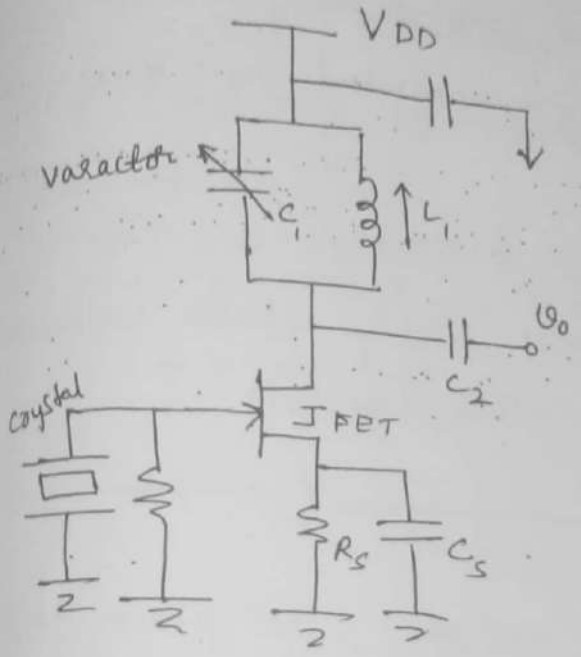
→ The inductance ~~and~~ L_1 and capacitor C_1

of the tank circuit are adjusted to the desired IS resonant frequency.

→ The o/p is taken at the drain of the JFET

→ The f/b in this case is provided by the drain-source capacitance.

CKt



Limitations

① The f/b is provided by the drain-source capacitance As different devices will have small variations in the values of C_{gd} and this may lead to variation in frequency.

② The o/p may be subject to amplitude variations due to load conditions.

→ To overcome the problem Dual gate MOSFET can be used.

Applications of crystal oscillators

→ High Q & stability are the main advantage of crystal oscillators.

→ Temperature compensated crystal oscillator finds use in many digital ICs.

→ Voltage controlled crystal oscillators are used in phase locked loop (PLL) circuits where the frequency is controlled by the external voltage.

→ Oven Controlled crystal oscillators are known to be most precise and highly stable oscillators. These are used in wireless systems.

Problems

1. In an RC phase shift oscillator, the phase shift network uses the resistances each of 4.7 KΩ and the capacitors each of 0.47 μF. Find the frequency of oscillations

Given $R = 4.7\ K\Omega$ & $C = 0.47\ \mu F$

$$\therefore f = \frac{1}{2\pi\sqrt{6}RC} = \frac{1}{2\times\pi\times\sqrt{6}\times 4.7\times10^{3}\times 0.47\times10^{-6}}$$

$$= 29.413\,Hz$$

Problems on Oscillators

In an RC phase-shift oscillator, $R = 200\,k\Omega$ & $C = 200\,pF$ find the frequency of the BJT-based oscillator.

$$f_0 = \frac{1}{2\pi RC\sqrt{6}}$$

$$f_0 = \frac{1}{2\times\pi\times 200\times10^{3}\times 200\times10^{-12}\sqrt{6}} = 1625\,Hz \text{ (or) } 1.625\,KHz$$

In a Colpitt's oscillator, $C_1 = C_2 = C$ & $L = 100\,\mu H$. The frequency of oscillations is 500 KHz. Determine value of C.

Given: $L = 100\,\mu H$, $C_1 = C_2 = C$ & $f = 500\,KHz$.

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$\Rightarrow C_{eq} = 1.0132\times10^{-9}\,F$$

$$C_{eq} = \frac{C_1 C_2}{C_1 + C_2} \quad \& \quad C_1 = C_2 = C.$$

$$C_{eq} = C/2$$

$$1.0132\times10^{-9} = \frac{C}{2} \Rightarrow C = 2.026\,nF$$

#4 Find the frequency of the oscillations of transistorized colpitts oscillator having tank circuit parameters as $C_1 = 150\,pF$, $C_2 = 1.5\,nF$ & $L = 50\,\mu H$

Soln

$$C_{eq} = C_1C_2/C_1+C_2 = 136.363\times10^{-12}\,F$$

$$f = \frac{1}{2\pi\sqrt{LC_{eq}}} = 1.927\,MHz$$

4. calculate the frequency of oscillations of a Hartley oscillator having $L_1 = 0.5\ mH$, $L_2 = 1\ mH$ & $C = 0.2\ \mu F$.

Sol^n $L_{eq} = L_1 + L_2 = \underline{1.5\ mH}$

$$f = \frac{1}{2\pi\sqrt{1.5\times10^{-3} \times 0.2\times10^{-6}}} = \underline{9.19\ KHz}$$

5. In a transistorized Hartley oscillator the two inductances are 2 mH & 20 μH. while the frequency is to be changed from 950 KHz to 2050 KHz. calculate the range over which the capacitor is to be varied.

Sol^n. $f = \frac{1}{2\pi\sqrt{C L_{eq}}}$

$L_{eq} = L_1 + L_2 = 0.00202$

$f = f_{max} = 2050\ KHz$

$\therefore C_{min} = \underline{2.98\ pF}$

$f = f_{min} = 950\ KHz$.

$C_{max} = 13.89\ pF$

Hence, C must be varied from 2.98 to 13.89 pF, to get the required frequency variation.

MOD-3

Feedback

Introduction —

Harold Black, an electronics engineer with the Western Electric Company, invented the feedback amplifier in 1928. Since then the technique has been widely used in electronic ckts either implicitly or explicitly. The concept of feedback and its associated theory are used in areas other than engineering also such as in the modeling of biological systems

7.1 The General Feedback Structure —

Following fig shows the basic structure of a feedback amplifier

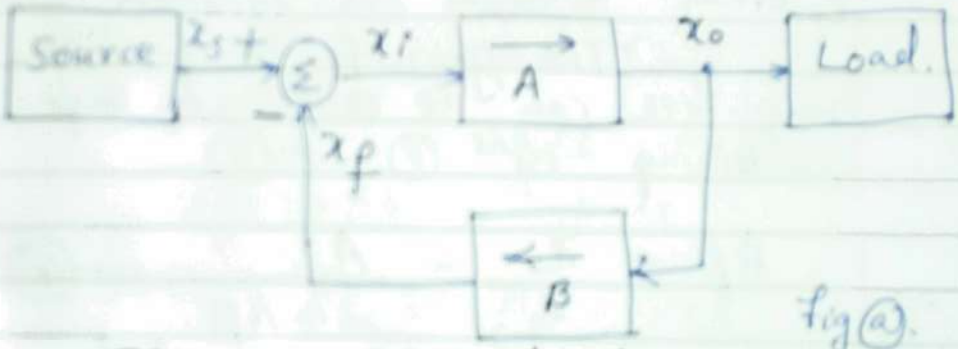


fig ②.

It is a signal-flow diagram, where each of the quantities x can represent either a voltage or a current signal. The open-loop amplifier has a gain A; thus the output x_o is related to the input x_i by

$$x_o = A x_i \quad \text{——— ①}$$

The output x_o is fed to the load as well as to a feedback network, which

produces a sample of the output. This sample x_f is related to x_o by the feedback factor β

$$x_f = \beta x_o \quad \text{---} (2)$$

The feedback signal x_f is subtracted from the source signal x_s which is the input to the complete feedback amplifier, to produce the signal x_i which is the input to the basic amplifier

$$\text{i.e } x_i = x_s - x_f \quad \text{---} (3)$$

Fig (a) above also implies that the forward transmission occurs entirely through the basic amplifier and the reverse transmission occurs entirely through the feedback network

The gain of the feedback amplifier can be obtained by combining eqn (1) to (3)

$$A_f = \frac{x_o}{x_s} = \frac{A}{1 + A\beta} \quad \text{---} (4)$$

The quantity $A\beta$ is called loop gain. For the feedback to be negative, the loop gain $A\beta$ should be positive; that is the feedback signal x_f should have the same sign as x_s, thus resulting in a smaller difference signal x_i.

Eqn (4) indicates that gain with feedback A_f will be smaller than the open-loop gain A

(3)

by the quantity $(1+AB)$, which is called the 'amount of feedback'

If the loop gain AB is large, $AB >> 1$, then

$$A_f \cong \frac{A}{AB} \cong \frac{1}{\beta} \quad \text{—— (5)}$$

That is gain of the feedback amplifier is almost determined by the feedback network.

Equations (1) to (3) can be combined to obtain the following expression for the feedback signal x_f as follows ——

we have $x_f = \beta \cdot x_o$

$$= \beta [A x_i]$$
$$= AB x_i$$
$$= AB [x_s - x_f]$$
$$= AB x_s - AB \cdot x_f$$
$$x_f [1+AB] = AB \cdot x_s$$
$$\therefore x_f = \frac{AB}{1+AB} \cdot x_s \quad \text{—— (6)}$$

Thus for $AB >> 1$, we see that $x_f \cong x_s$ which implies that the signal x_i at the input of the basic amplifier is reduced to almost zero. Thus if a large amount of -ve feedback is employed, the feedback signal x_f becomes an almost identical replica of the input signal x_s.

An outcome of this property is the tracking of the two I/P

terminals of an op-amp. The difference between x_s & x_f which is x_i is sometimes referred to as the "error signal". Accordingly the input differencing ckt is also called a 'comparison ckt'

An expression for x_i can be determined as follows —

We have from (2)

$$x_o = A \cdot x_i$$

or $$x_i = x_o / A \quad \text{—— (7)}$$

From (2) we have

$$x_f = \beta x_o$$

$$\therefore x_o = \frac{x_f}{\beta}$$

Substituting in (7) we get

$$x_i = \frac{x_f/\beta}{A}$$

$$= \frac{x_f}{A\beta} \quad \text{— (8)}$$

From (3) we have:

$$x_i = x_s - x_f$$

$$\therefore x_f = x_s - x_i$$

Substitute in (8)

$$x_i = \frac{x_s - x_i}{A\beta}$$

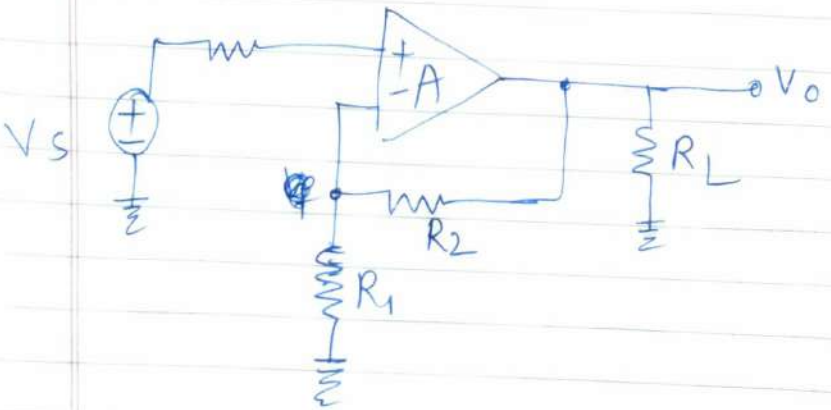
$$A\beta x_i = x_s - x_i$$

$$x_i [1 + A\beta] = x_s$$

$$\text{or } x_i = \frac{x_s}{1+A\beta} \quad \text{— (a)}$$

From eqn (a) we can verify that if $A\beta >> 1$, x_i becomes very small. Observe that -ve feedback reduces the signal that appears at the input terminals of the basic amplifier by the amount of feedback, $(1+A\beta)$.

Ex-7.1 The non inverting op-amp with feedback is shown in following fig



(a) Assume that the op-amp has ∞ I/P resistance and zero output resistance. Find an expression for the feedback factor β.

(b) If the open-loop gain $A = 10^4$ find R_2/R_1 to obtain a closed-loop voltage gain A_f of 10.

(c) What is the amount of feedback in decibels?

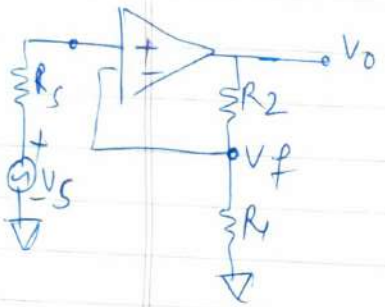
(d) If $V_s = 1V$, find V_o, V_f and V_i.

(e) If A decreases by 20%, what is the corresponding decrease in A_f?

(6)

(a) Feedback voltage V_f is the drop developed across R_1 resistor.

Applying Vg divider rule



$$V_f = \frac{R_1 V_o}{R_1 + R_2}$$

$$\frac{V_f}{V_o} = \beta = \frac{R_1}{R_1 + R_2} \;//$$

(b) $A = 10^4$

$A_f = 10.$

$\frac{R_2}{R_1} = ?$

$$A_f = \frac{A}{1 + A\beta}$$

$$1 + A\beta = \frac{A}{A_f} = \frac{10^4}{10} = 10^3$$

$$A\beta = 10^3 - 1$$

$$= 999$$

$$\beta = \frac{999}{10^4} = 0.0999$$

$$\frac{1}{1 + \frac{R_2}{R_1}} = 0.0999$$

$$1 = 0.0999 + 0.0999 \frac{R_2}{R_1}$$

$$\therefore \frac{R_2}{R_1} = \frac{1 - 0.0999}{0.0999}$$

$$= 9.01 \;//$$

(7)

(c) Amount of feedback in dB?

Amount of feedback = $(1+AB)$

$= 1 + 10^4 \times 0.0999$

$= 1 + 999$

$= 1000$

In dB $= 20 \log_{10}(1+AB)$

$= 20 \log_{10}(1000)$

$= 20 \times 3$

$= 60$ dB //

(d) If $V_s = 1V$ find V_o, V_f & V_i

$V_o = A_f \cdot V_s$

$= 10 \times 1V = 10V$

$V_f = \beta V_o$

$= 0.0999 \times 10$

$= 0.999\ V.$

$V_i = V_s - V_f$

$= 1 - 0.999V$

$= 0.001V.$

(e) A is decreased by 20%. % decrease in A_f = ?

$A = 10^4 - 20\%$ of 10^4

$= 10^4 - \frac{20}{100} \times 10^4$

$= 10^4 - 2000$

$= 8000.$

7.2 Some Properties of Negative Feedback

In amplifier design, negative feedback is applied to effect one or more of the following properties

1. Desensitize the gain: That is make the value of the gain less sensitive to variations in the value of ckt components, such as might be caused by changes in temperature.
2. Reduce Nonlinear Distortion: That is make the output ∝ to the input. In other words, make the gain constant, independent of signal level.
3. Reduce the effect of noise: That is minimize the contribution to the output of unwanted electric signals generated either by the ckt components themselves or by interference.
4. Control the input and output impedances: That is raise or lower the input and output impedances by the selection of an appropriate feedback topology
5. Extend the bandwith of the amplifier.

Note all of the desirable properties mentioned above are obtained at the expense of reduction in gain.

In the following we consider some of these properties in more detail.

(9)

7.2.1 Gain Desensitivity

This sensitivity-reduction property can be analytically established as follows —

Assume that β is constant we have

$$A_f = \frac{A}{1+A\beta} \quad \text{—(1)}$$

Taking differentials of eq^n (1) both sides results in

$$dA_f = \frac{dA}{(1+A\beta)^2} \quad \text{—(2)}$$

Dividing eq^n (2) by eq^n (1) yields

$$\frac{dA_f}{A_f} = \frac{1}{(1+A\beta)} \frac{dA}{A} \quad \text{—(3)}$$

which says that the percentage change in A_f is smaller than the percentage change in A by the amount of feedback. For this reason the amount of feedback, $(1+A\beta)$ is also known as the desensitivity factor.

7.2.2 Bandwidth Extension.

Consider an amplifier whose high freq response is characterized by a single pole. Its gain at mid and high freqs can be expressed as

$$A(s) = \frac{A(s)}{1+\beta A(s)}$$

$$A(s) = \frac{A_M}{1 + s/\omega_H} \quad \text{---} (4)$$

where A_M denotes the midband gain and ω_H is the upper 3dB freq.

Application - ve feedback, with a frequency - independent factor β, around this amplifier results in a closed loop gain $A_f(s)$ given by

$$A_f(s) = \frac{A(s)}{1 + \beta A(s)}$$

Substituting for $A(s)$ from eqn (4) results in

$$A_f(s) = \frac{A_M/(1+s/\omega_H)}{1 + \beta\left[A_M/(1+s/\omega_H)\right]}$$

$$= \frac{A_M/(1+s/\omega_H)}{\frac{(1+s/\omega_H) + \beta A_M}{(1+s/\omega_H)}}$$

$$= \frac{A_M}{(1+\beta A_M) + s/\omega_H}$$

$$= \frac{A_M/(1+A_M\beta)}{1 + s/\omega_H(1+A_M\beta)} \quad \text{---} (5)$$

Thus the feedback amplifier will have a midband gain of $A_M/(1+A_M\beta)$ and an upper 3-dB freq ω_{Hf} given by

$$\omega_{Hf} = \omega_H(1 + A_M\beta) \quad \text{---} (6)$$

(11)

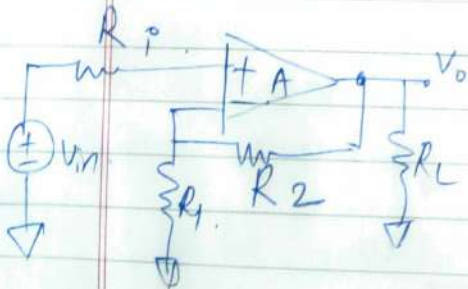
It follows that the upper 3-dB freq is increased by a factor equal to the amount of feedback.

Similarly it can be shown that if the open-loop gain is characterized by a dominant low-freq pole giving rise to a lower 3-dB freq ω_L, then feedback amplifier will have a lower 3-dB freq ω_{Lf} as-

$$\omega_{Lf} = \frac{\omega_L}{1 + A_M \beta} \quad \text{---} \quad (7)$$

Note that the amplifier bandwidth is increased by the same factor by which its midband gain is decreased, maintaining the gain-bandwidth product at a constant value.

EX 7.2 Consider the non-inverting op-amp ckt of example 7.1. Let the open loop gain A have a low freq value of 10^4 and a uniform -6dB/octave roll off at high frequencies with a 3-dB frequency of 100Hz. Find the low-freq gain and the upper 3dB freq of a closed loop amplifier with $R_1 = 1k\Omega$ and $R_2 = 9k\Omega$



$R_1 = 1K\Omega$, $R_2 = 9K\Omega$

$A = 10^4$

$f_H = 100Hz$.

$$\beta = \frac{R_1}{R_1 + R_2} = \frac{1}{1 + \frac{R_2}{R_1}}$$

$$= \frac{1}{1 + \frac{9k}{1k}} = \frac{1}{10} = 0.1$$

(12)

$$A_f(s) = \frac{A(s)}{1+\beta A(s)}$$

$$= \frac{10^4}{1+0.1\times 10^4}$$

$$= 9.99$$

We have

$$\omega_{Hf} = \omega_H (1+A_M\beta)$$

$$2\pi f_{Hf} = 2\pi f_H (1+A_M\beta)$$

$$f_{Hf} = f_H (1+A_M\beta)$$

$$= 100(1+10^4\times 0.1)$$

$$= 100100$$

$$= 100.1\,kHz$$ //

7.2.3 Noise Reduction.

Negative feedback can be employed to reduce the noise or interference in an amplifier or more precisely, to increase the ratio of signal to noise ratio.

This noise reduction process is possible only under certain conditions.

Consider the situation shown in fig (a) below

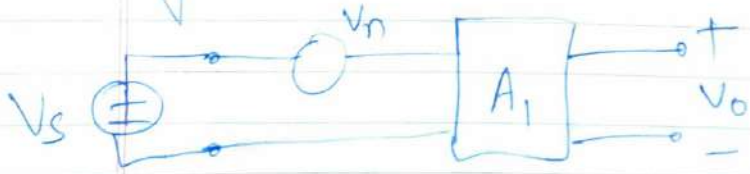


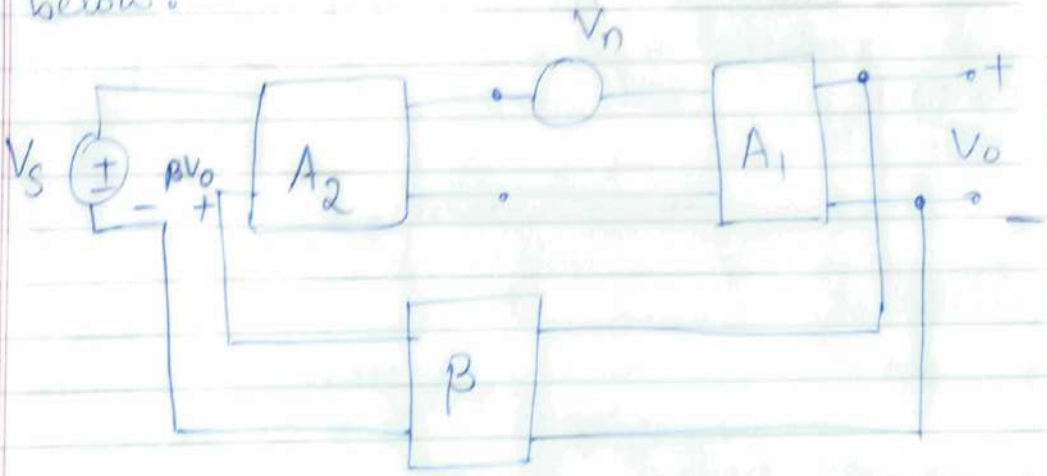
fig (a)

Fig (a) shows an amplifier with gain A_1, an i/p signal V_s, and noise & interference V_n

It is assumed that for some reason this amplifier suffers from noise and that the noise can be assumed to be introduced at the input of the amplifier. The signal-to-noise ratio for this amplifier is

$$\frac{S}{N} = \frac{V_s}{V_n} \qquad \text{---------- (1)}$$

Consider next the ckt in fig (b) shown below:



Here we assume that it is possible to build another amplifier stage with gain A_2 that does not suffer from noise problem. If this is the case, then the original amplifier A_1 can be preceded by clean amplifier A_2 and apply -ve feedback around the overall cascade.

The output voltage of the ckt can be found by superposition —

(14)

$$V_o = V_s \cdot \frac{A_1 A_2}{1 + A_1 A_2 \beta} + V_n \frac{A_1}{1 + A_1 A_2 \beta} \quad \text{---(8)}$$

Thus the signal to noise ratio at the output becomes

$$\frac{S}{N} = \frac{V_s}{V_n} A_2 \quad \text{---(9)}$$

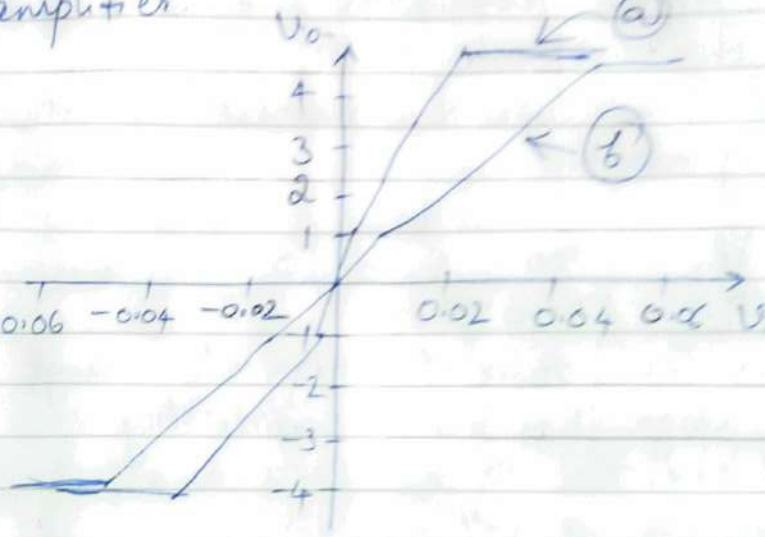
which is A_2 times higher than in the original case.

This technique is usually used in output power amplifier stage of an audio amplifier. Here the 'power supply hum' is reduced by using a preamplifier

Ex 7.3

7.2.4 Reduction in Nonlinear Distortion —

In the following fig, curve (a) shows the transfer characteristic of an amplifier



As indicated, the characteristic is piecewise linear, with the voltage gain changing from 1000 to 100 and then to 0. Thus it generates a large amount of nonlinear distortion

The amplifier transfer characteristic can be considerably linearized through the application of negative feedback. This is because the -ve feedback reduces the dependence of the overall closed-loop amplifier gain on the open-loop gain of the basic amplifier. Thus large changes in open-loop gain give rise to much smaller corresponding changes in the closed loop gain.

To illustrate apply -ve feedback with $\beta = 0.01$ to the amplifier whose Char. shown by curve (a) in above fig. The resulting transfer characteristic is shown in curve (b).

(16)

Here the slope of the steepest segment is given by

$$A_{f_1} = \frac{1000}{1 + 1000 \times 0.01} = 90.9$$

and the slope of the next segment is given by

$$A_{f_2} = \frac{100}{1 + 100 \times 0.01} = 50.$$

Thus the order of magnitude change in slope has been considerably reduced. The price paid is a reduction in voltage gain.

7.3 The four basic feedback topologies.

Based on the quantity to be amplified (V_g or current) and on the desired form of output (V_g or current), amplifiers can be classified into four categories.

7.3.1 Voltage Amplifiers

Voltage amplifiers are intended to amplify an input voltage signal and provide an output voltage signal. It is essentially a voltage controlled voltage source.

Here the signal source is represented in terms of Thevenin's equivalent ckt. The feed back network should sample output voltage. The feedback signal x_f is mixed with source v_g in series.

A suitable feedback topology for the voltage amplifier is the 'voltage-mixing - voltage-sampling' as shown in fig (a) below. Because of the series connection at the input and the parallel or shunt connection at the output, this feedback topology is also known as 'series-shunt feedback'.

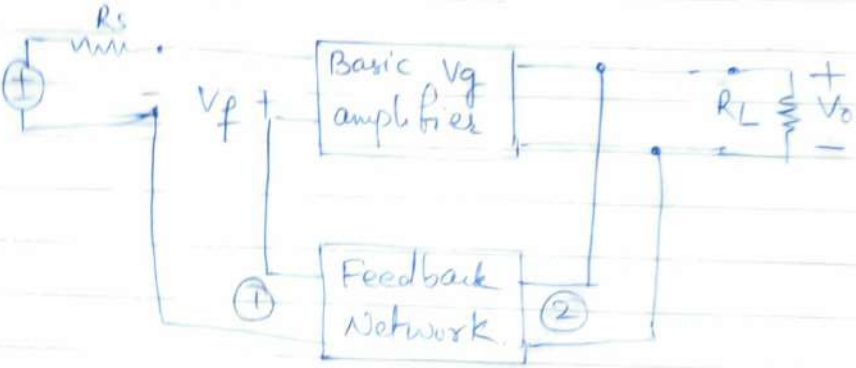


fig (a)

This topology not only stabilizes the voltage gain but also results in a higher input resistance and a lower output resistance.

1.3.2 Current Amplifiers

The input signal in a current amplifier is essentially a current, and thus the signal source is most conveniently represented by its Norton equivalent. The output quantity of interest is current; hence the feedback network should sample the output current. The feedback signal should be in current form so that it may be mixed in shunt with the source current. Thus the feedback topology suitable for a

(18)

current amplifier is the 'current-mixing current-sampling topology as shown in fig (b) below. Because of the parallel (or shunt) connection at the input, and the series connection at the output, this feedback topology is also known as 'shunt-series feedback'

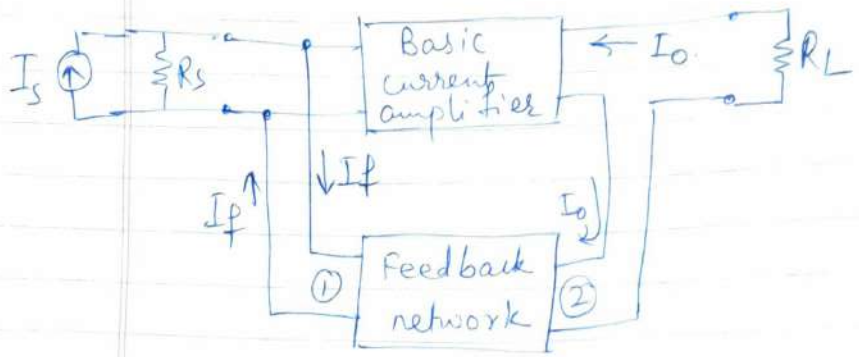


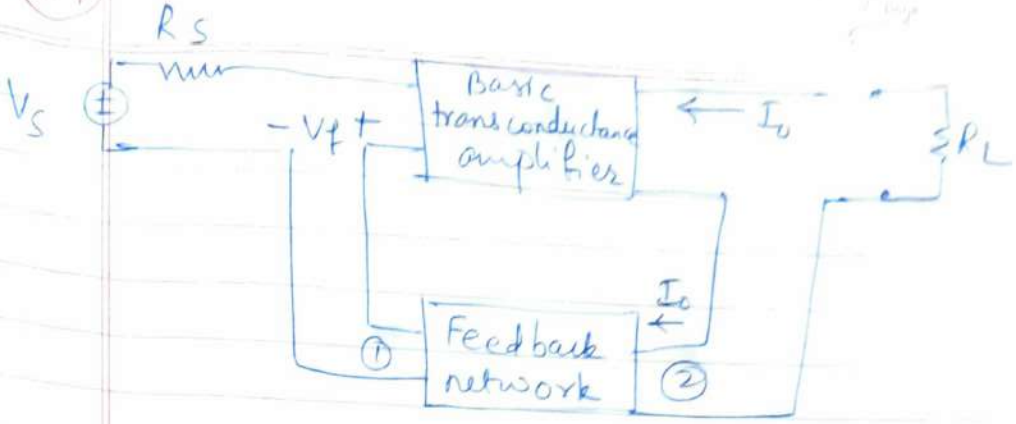
fig (b)

This topology not only stabilizes the current gain but also results in a lower input resistance and a higher output resistance, both desirable properties for a current amplifier

7.3.3 Transconductance Amplifiers -

In transconductance amplifiers the input signal is a voltage and the output signal is a current. It follows that the appropriate feedback topology is the 'voltage-mixing current-sampling' topology as shown in fig (c) below. The presence of the series connection at both the input and the output gives this feedback topology the alternative name 'series-series feedback'

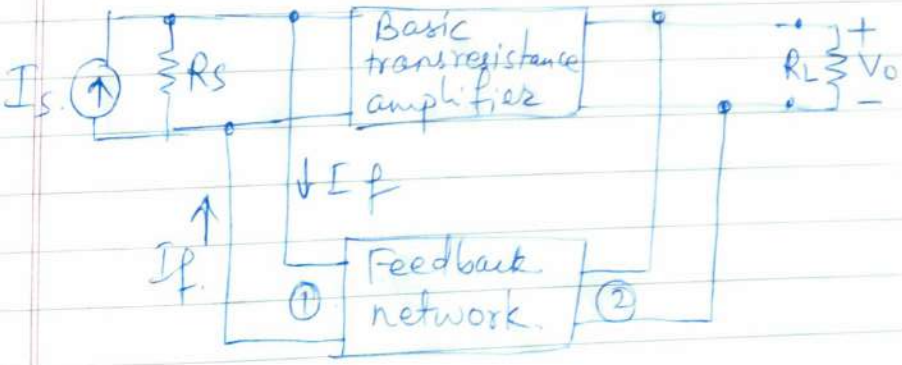
(19)



7.3.4 Transresistance Amplifier

In transresistance amplifiers the input signal is current and the output signal is voltage It follows that the appropriate feedback topology is of the 'current-mixing voltage-sampling' type shown in fig (d) below.

The presence of the parallel (or shunt) connection at both the input and the output makes this feedback topology also known as 'shunt-shunt feedback'



7.4 The Series - Shunt Feedback Amplifier

7.4.1 The Ideal Situation --

The ideal structure of the series-shunt feedback amplifier is shown in fig @ below

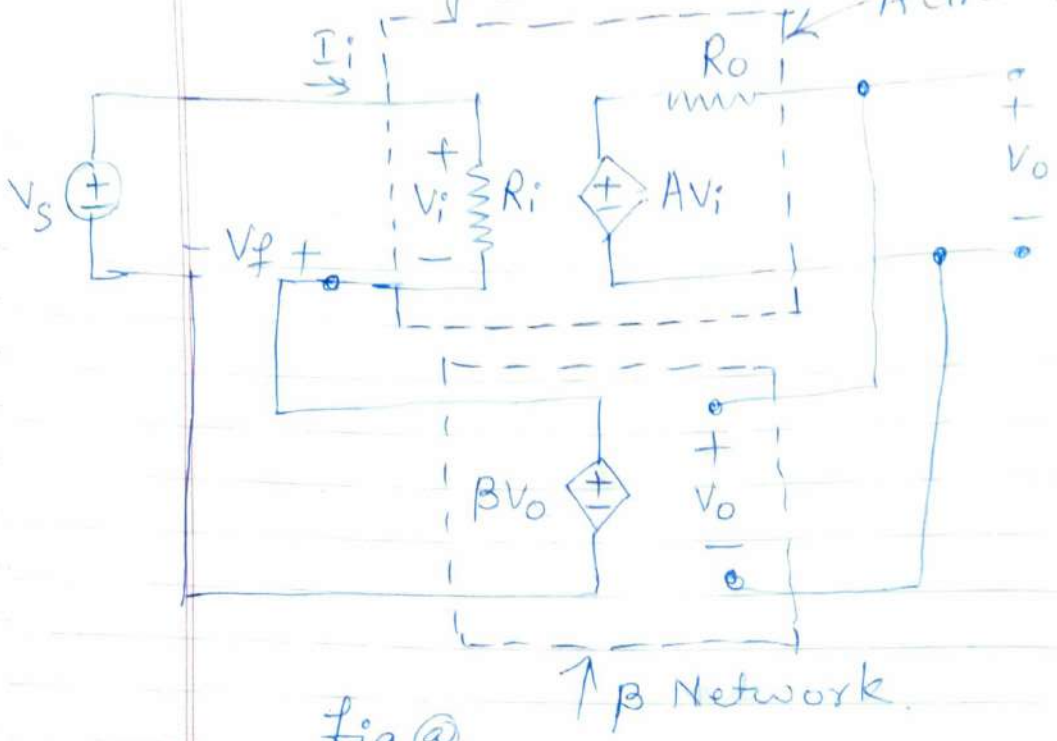


fig @

It consists of a 'unilateral' open-loop amplifier (The A ckt) and an ideal voltage mixing voltage sampling feedback network (The β ckt)

The A ckt has an i/p resistance R_i, a voltage gain A and an output resistance R_o. It is assumed that the source and load resistances have been included inside the A ckt. Furthermore the β ckt does not load the A ckt, that is, connecting the β ckt does not change the value of A.

The ckt of fig @ exactly follows the ideal feedback model.

Therefore the closed-loop voltage gain A_f is given by

$$A_f = \frac{V_o}{V_s} = \frac{A}{1+A\beta} \quad \text{---(1)}$$

Note that A & β have reciprocal units, resulting in a dimensionless loop gain Aβ.

The equivalent ckt model of the series-shunt feedback amplifier is shown in fig (b) below.

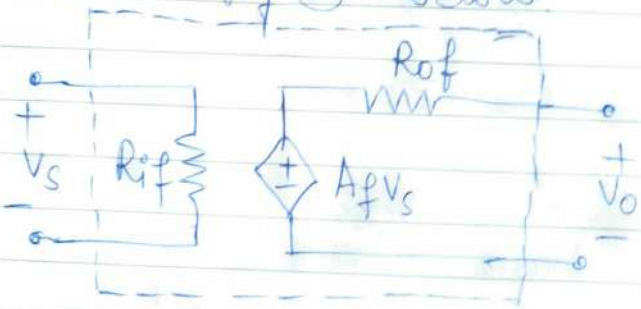


fig (b)

Here R_{if} and R_{of} denote the input and output resistances with feedback.

The relationship between R_{if} and R_i can be established by considering the ckt in fig (a).

$$R_{if} = \frac{V_s}{I_i} = \frac{V_s}{V_i/R_i}$$

$$= R_i \frac{V_s}{V_i}$$

$$= R_i \cdot \frac{V_i + \beta V_o}{V_i}$$

$$= R_i \frac{(V_i + A\beta V_i)}{V_i}$$

$$= R_i (1 + A\beta) \quad \text{---(2)}$$

(22)

That is, in this case the -ve feedback increases the input resistance by a factor equal to the amount of feedback. Since the derivation above does not depend on the method of sampling (shunt or series), it follows that the relationship between R_{if} and R_i is a function only of the method of mixing.

Finally, it should be pointed out that eqn (2) can be generalized to the form

$$Z_{if} = Z_i(s)\left[1 + A(s)\beta(s)\right] \quad -(3)$$

To find the output resistance R_{of} of the feedback amplifier in fig (a), we reduce V_s to zero and apply a test voltage V_t at the output as shown in fig (c) below.

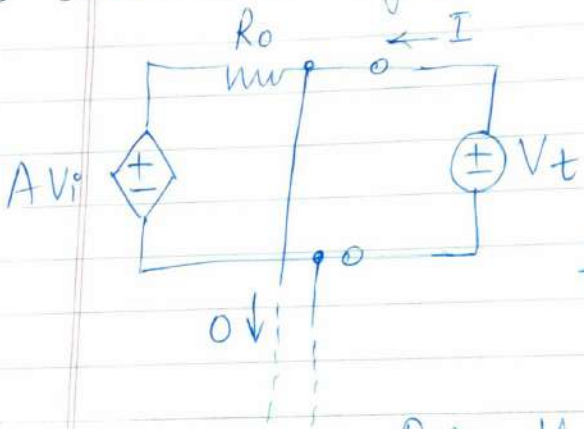


fig (c)

$$R_{of} = \frac{V_t}{I}$$

From fig (c), we can write

$$-V_t + R_o I + A V_i = 0$$

$$R_o I = V_t - A V_i$$

$$I = \frac{V_t - A V_i}{R_o} \quad -(4)$$

(23)

and since $V_s = 0$, from fig (a)

$$V_i = -V_f$$

$$= -\beta V_o$$

$$= -\beta V_t$$

substituting in eqn (4) we get

$$I = \frac{V_t + A\beta V_t}{R_o}$$

Thus

$$R_{of} = \frac{V_t}{V_t(1+A\beta)/R_o}$$

$$= \frac{R_o}{1+A\beta} \quad \text{---(5)}$$

That is, the -ve feedback in this case reduces the output resistance by a factor equal to the amount of feedback.

It can be noted that eqn (5) derivation does not depend on the method of mixing. Thus the relationship between R_{of} and R_o depends only on the method of sampling.

Finally eqn (5) can be generalized to

$$Z_{of}(s) = \frac{Z_o(s)}{1+A(s)\cdot\beta(s)} \quad \text{---(6)}$$

7.5 The Series-Series Feedback Amplifier

7.5.1 The Ideal Case

The series-series feedback topology stabilizes I_o/V_s and is therefore best suited for transconductance amplifiers. Fig (a) shows the ideal structure for the series-series feedback amplifier below.

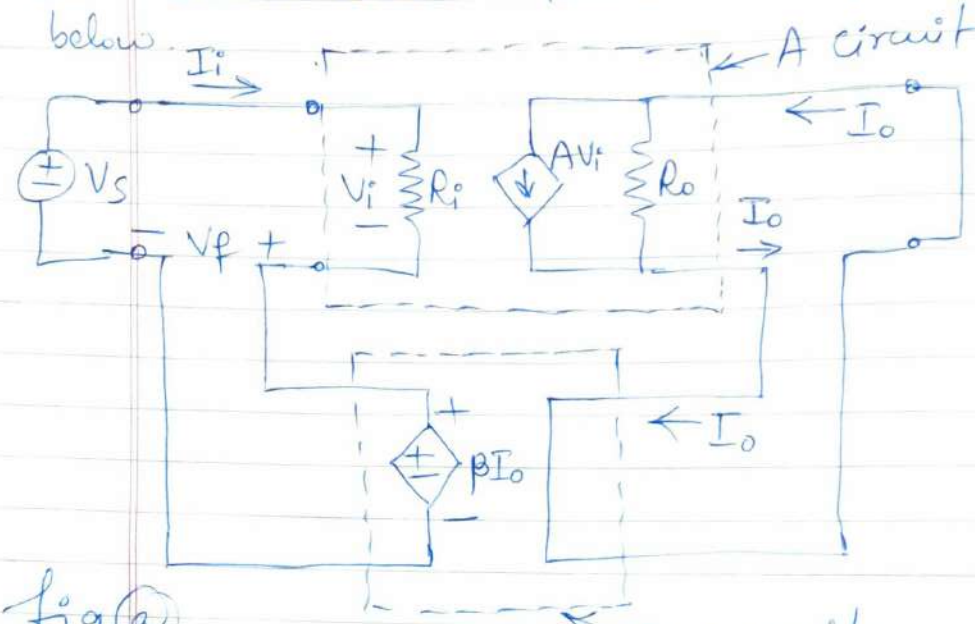


fig (a)

It consists of a unilateral open-loop amplifier (The A ckt) and an ideal feedback network. Note that in this case A is a transconductance.

$$A = \frac{I_o}{V_i} \quad \text{—— (1)}$$

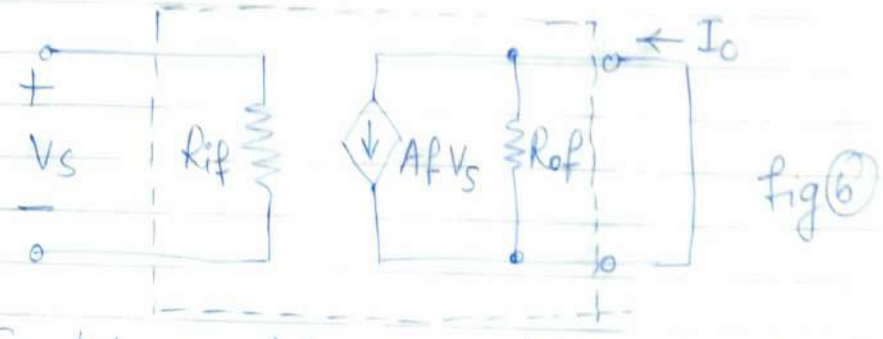
while β is a transresistance. Thus the loop-gain Aβ remains a dimensionless quantity.

In fig (a) the load and source resistances have been absorbed inside the A ckt, and the β ckt does not load the A ckt. Thus the

follows the ideal feedback model and we can write

$$A_f = \frac{I_o}{V_s} = \frac{A}{1+A\beta} \quad \text{---(2)}$$

This transconductance with feedback is included in the equivalent ckt model of the feedback amplifier shown in fig(b)



fig(b)

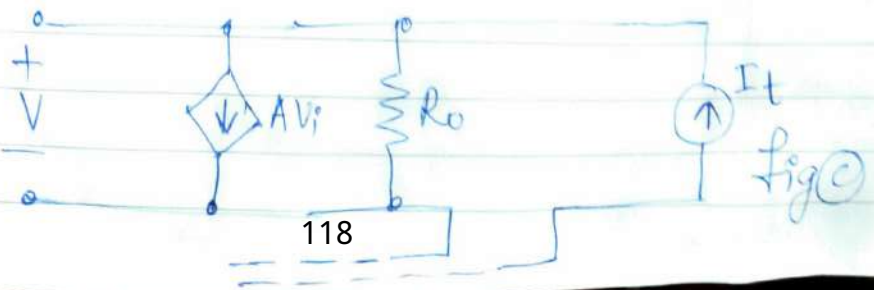
In this model, R_{if} is the input resistance with feedback and is given by

$$R_{if} = R_i(1+A\beta) \quad \text{---(3)}$$

The relationship between R_{if} and R_i is a function of only the method of mixing

Note that Voltage (or series) mixing always increases the input resistance

To find the output resistance R_{of} we reduce V_s to zero and break the output ckt to apply a test current I_t as shown in fig(c)



fig(c)

(26)

$$R_{of} = \frac{V}{I_s} \quad \text{— (3)}$$

In this case

$$V_p = -V_f$$

$$= -\beta I_o$$

$$= -\beta I_t$$

Thus for the ckt- in fig (c), we obtain

$$V = (I_t - AV_i) R_o$$

$$= (I_t + A\beta I_t) R_o$$

$$R_{of} = (1 + A\beta) R_o \quad \text{— (4)}$$

That is in this case the -ve feedback increases the output resistance.

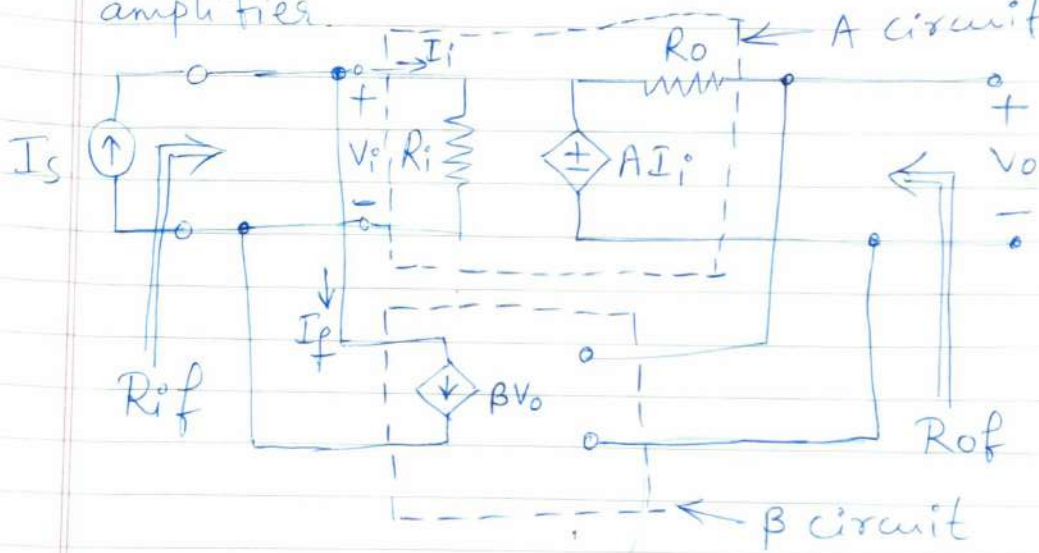
The relationship between R_{of} and R_o is a function only of the method of sampling. Note that the current (series) sampling increases it.

7.6 The Shunt-Shunt AND Shunt-Series Feedback Amplifiers

The methods of sections 7.4 & 7.5 can be extended to other two feedback topologies

7.6.1 The Shunt-Shunt Configuration

Following fig (a) shows the ideal structure for a shunt-shunt feedback amplifier.



Here the A ckt has an input resistance R_i, a transresistance A and an output resistance R_o. The β circuit is a voltage-controlled current source, and β is a transconductance.

The closed-loop gain A_f is defined as

$$A_f = \frac{V_o}{I_s} \quad \text{---(1)}$$

And is given by

$$A_f = \frac{A}{1+A\beta}$$

The i/p resistance with feedback is given by—

$$R_{if} = \frac{R_i}{1+A\beta} \quad \text{---(2)}$$

(23)

Note that the shunt connection at the input results in a reduced input resistance. Further the resistance Rif is the resistance seen by the source Is and it includes any source resistance.

The output resistance with feedback is given by

$$R_{of} = \frac{R_o}{1+AB} \quad \text{——— (3)}$$

where we note that the shunt connection at the output results in a reduced output resistance. This resistance includes any load resistance.

7.6.2 An Important Note

The methods employed for the analysis of feedback amplifiers are based on two assumptions —

Most of the forward transmission occurs in the basic amplifier and most of the reverse transmission (feedback) occurs in the feedback network.

For each of the 3 topologies considered thus far, these two assumptions were mathematically expressed as conditions on the relative magnitudes of the forward and reverse two-port parameters of the basic amplifier and the feedback network.

7.6.3 The Shunt Series Configuration

Fig @ below shows the ideal structure of the shunt-series feedback amplifier

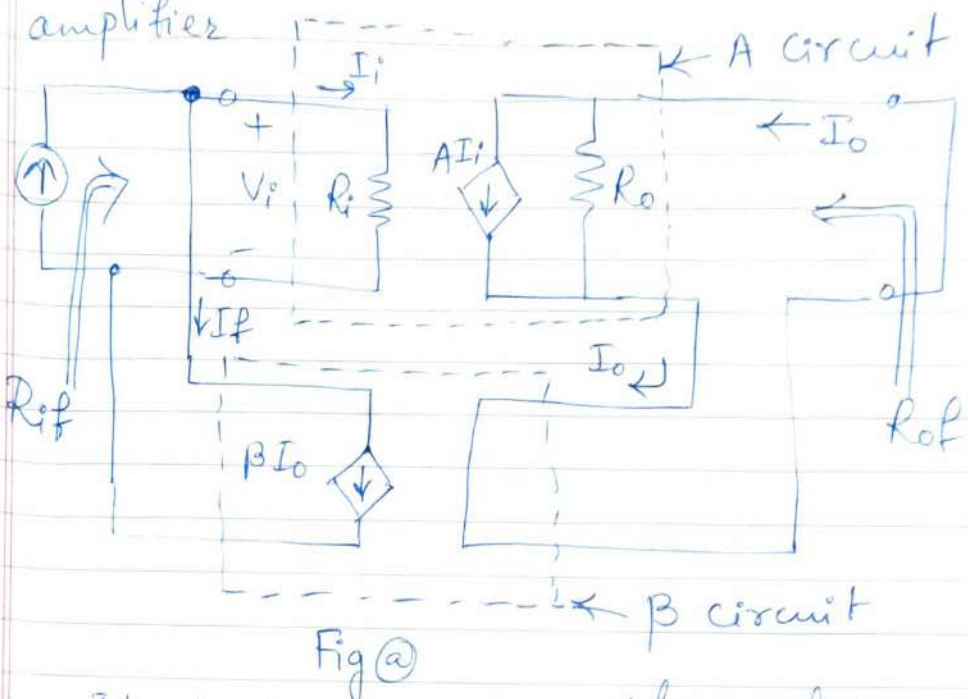


Fig @

It is a current amplifier whose gain with feedback is defined as

$$A_f = \frac{I_o}{I_s} = \frac{A}{1+A\beta} \quad \text{— (1)}$$

The input resistance with feedback is the resistance seen by the current source I_s and is given by

$$R_{if} = \frac{R_i}{1+A\beta} \quad \text{— (2)}$$

Again we note that the shunt connection at the input reduces the input resistance.

The output resistance with feedback is the resistance seen by looking between the two terminals from o/p side

This resistance is given by

$$R_{of} = R_o(1+A\beta) \quad \text{— (3)}$$

We note that the increase in output resistance is due to the current (series) sampling.

(31)

12.1 Output Stages and Power Amplifiers

Introduction.

An important function of the output stage is to provide the amplifier with a low output resistance so that it can deliver the output signal to the load without loss of gain. Since the output stage is the final stage of the amplifier, it usually deals with relatively large signals. Linearity remains a very important requirement. The measure of goodness of the design of the output stage is the "total harmonic distortion" (THD) that it introduces. This is the rms value of the harmonic components of the output signal, excluding the fundamental, expressed as a percentage of the rms of the fundamental

A power amplifier is simply an amplifier with a high-power output stage.

Classification of Output Stages.

Output stages are classified according to the collector current waveform that results when an input signal is applied.

The 'class A' stage, whose associated waveform is shown in fig (a) below.

(32)

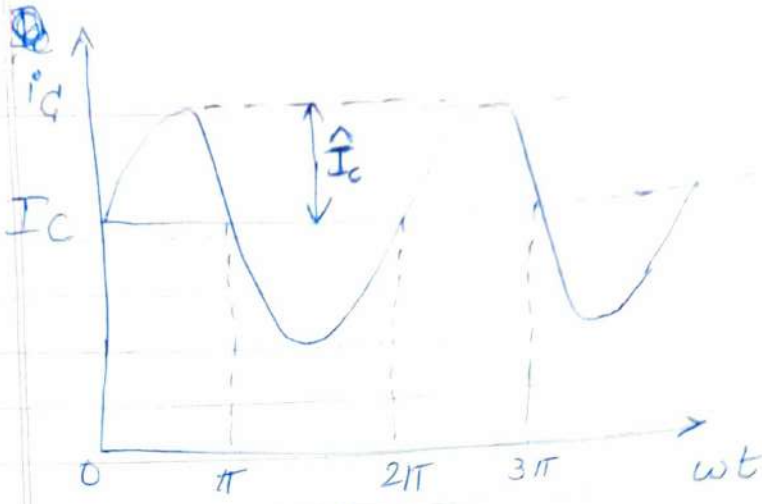


fig (a)

It is biased at a current I_C greater than the amplitude of the signal current $\hat{I}_c$. Thus the transistor in a class A stage conducts for the entire cycle of the input signal, that is, the conduction angle is 360°. These amplifiers are only useful with sinusoidal inputs of small amplitudes. Their power efficiency is low (30%)

The class-B stage, whose associated waveform is shown in fig (b), is biased at zero dc current.

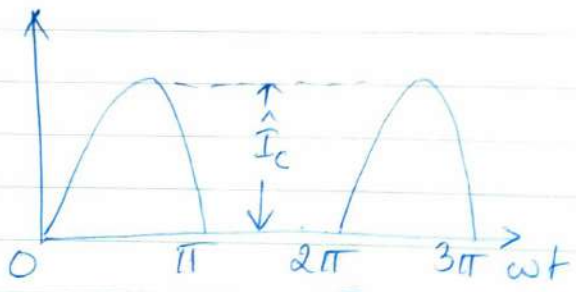


fig (b)

Thus a transistor in a class-B stage conducts for only half the cycle of the input sine wave,

resulting in a conduction angle of 180°.

An intermediate class between A and B, called class AB involves biasing the transistor at a nonzero dc current much smaller than the peak current of the sine-wave signal. As a result the transistor conducts for an interval slightly greater than half a cycle as shown in fig (c) below.

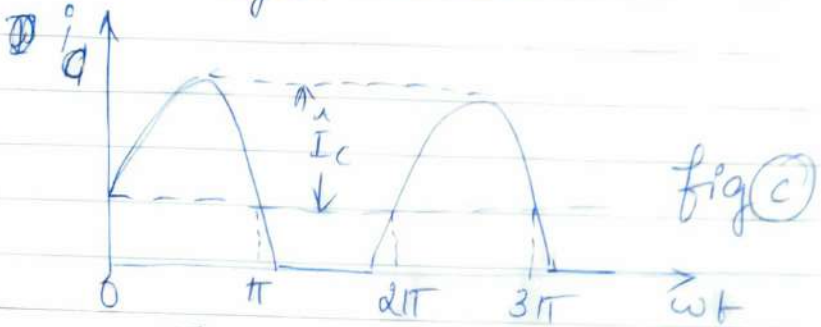


fig (c)

The resulting conduction angle is greater than 180° but much less than 360°. The class AB stage has another transistor that conducts for an interval slightly greater than that of the negative half-cycle and the currents from the two transistors are combined in the load. It follows that near the zero crossings of the input sinusoid, both transistors conduct. Class B and class C amplifiers have power efficiencies over 78% but are also limited by linear mode operation.

Fig (d) below shows the collector-current waveform for a transistor operated as a class C amplifier.

(34)

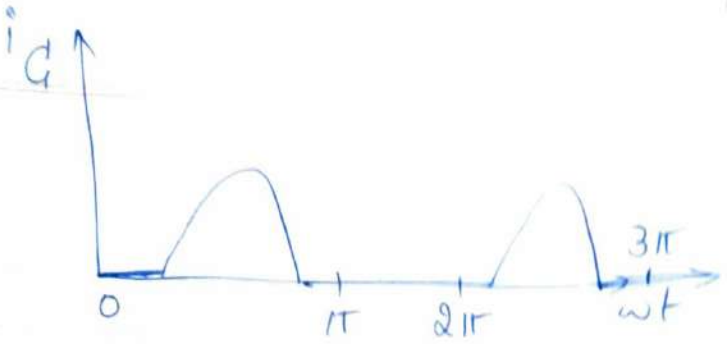


fig (d).

Observe that the transistor conducts for an interval shorter than that of a half-cycle; that is the conduction angle is less than 180°. The result is the periodically pulsating current waveform as shown. To obtain a sinusoidal output voltage, this current is passed through a parallel LC ckt, tuned to the freq of the Pyput sinusoid. The tuned ckt acts as a bandpass filter and provides an output voltage proportional to the amplitude of the fundamental component in the Fourier-Series representation of the current waveform.

For applications such as base stations of mobile communications where larger power output with higher power efficiency is required, one opts for switched mode power amplifiers (SMPAs). Their power efficiency is greater than 80%.

12.2 Class-A Output Stage

Because of the low output resistance, the emitter follower is the most popular class A output stage.

12.2.1 Transfer Characteristic

Fig ① below shows an emitter follower Q_1 biased with a constant current I supplied by transistor Q_2.

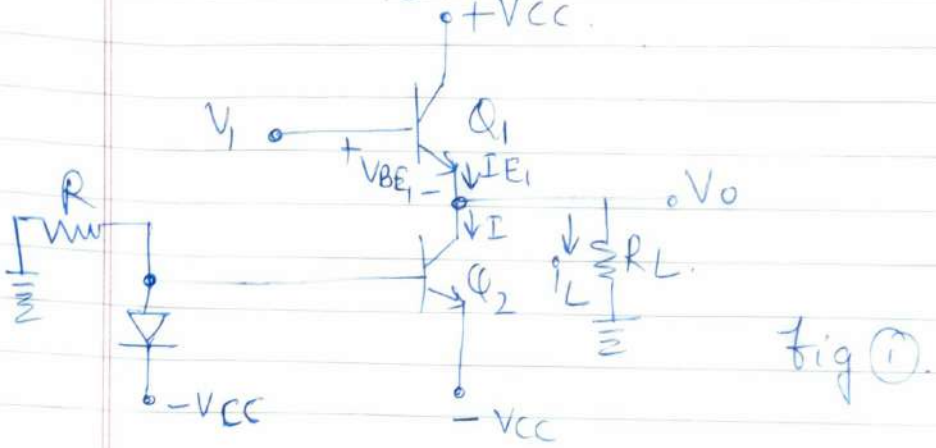


fig ①.

From the above fig,

$$I_{E_1} = I + i_L$$

The bias current I must be greater than the largest negative load current. Otherwise Q_1 cuts-off and class A operation will no longer be maintained.

The transfer characteristic of the emitter follower of above fig is described by

$$-V_I + V_{BE_1} + V_o = 0$$

$$\text{or } V_o = V_I - V_{BE_1} \quad \text{---} \quad ①$$

where V_{BE_1} depends on the emitter current I_{E_1} and hence on the load current i_L.

If we neglect the relatively small changes in v_{BE_1}, then the linear transfer curve shown in fig (2) results

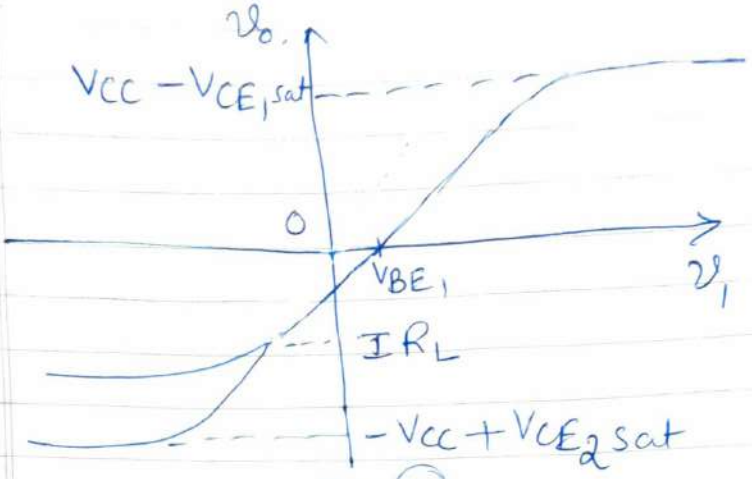


Fig (2)

As indicated the positive limit of the linear region is determined by the saturation of Q_1.

Thus $v_{o\,max} = V_{CC} - V_{CE_1 sat}$ — (2)

In the negative direction depending on the values of I and R_L, the limit of the linear region is determined either by Q_1 turning-off or by Q_2 saturating.

In the first case

$v_{o\,min} = -IR_L$ — (3)

if in the second case

$v_{o\,min} = -V_{CC} + V_{CE_2 sat}$ — (4).

The absolutely lowest output voltage is given by eq^n (4) and is achived if the bias current I is greater than the magnitude of the corresponding load current

$I \geq \dfrac{|-V_{CC} + V_{CE_2 sat}|}{R_L}$ — (5)

(31)

12.2.2 Signal Waveforms

From fig (2) if the bias current I is properly selected, neglecting $V_{CE\,sat}$, the output voltage can swing from $-V_{CC}$ to $+V_{CC}$ with the quiscent value being zero as shown in fig (3) below

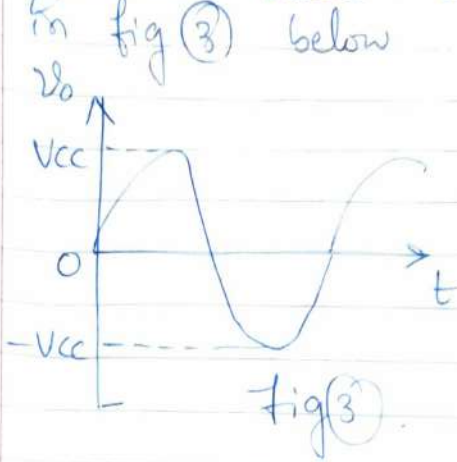


fig (3)

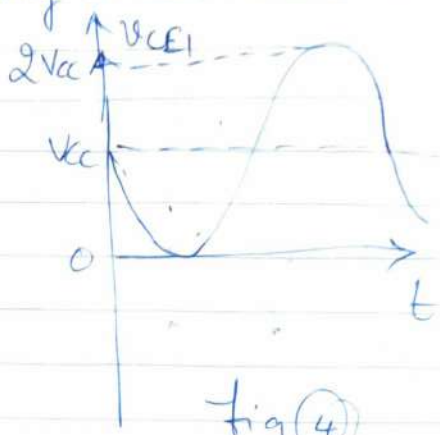


fig (4)

Fig (4) shows the corresponding waveform of

$$v_{CE_1} = V_{CC} - v_o.$$

Now assuming that the bias current I is selected to allow a maximum negative load current of V_{CC}/R_L, the collector current of Q_1 will have the waveform as shown in fig (5)

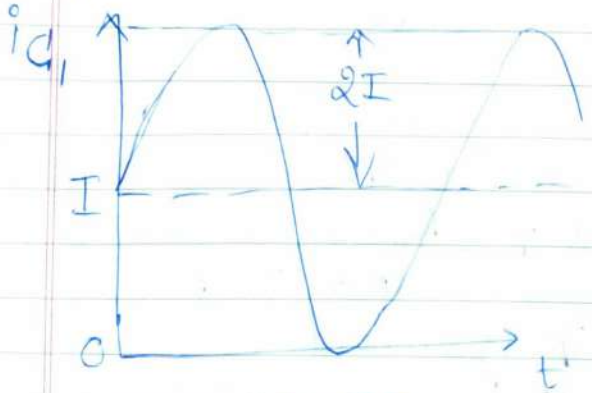


fig (5)

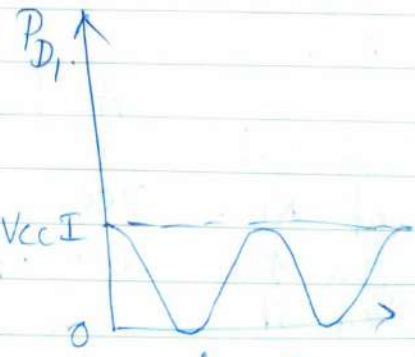


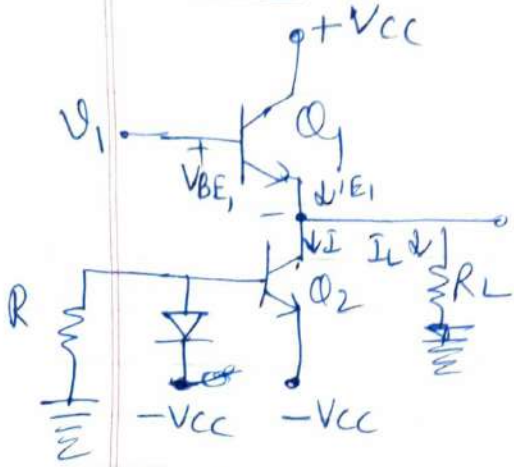
fig (6)

Finally fig (6) shows waveform of the instantaneous power dissipation in Q_1

$$P_{D_1} = v_{CE_1} \cdot i_{C_1} \quad \text{—— (6)}$$

12.2.3 ## Power Dissipation

In the waveforms above, fig (6) indicates that the maximum instantaneous power dissipation in Q_1 is $V_{CC}I$. This is equal to the quiescent power dissipation in Q_1.



The power dissipation in Q_1 depends on the value of R_L.

Consider the extreme case of an output open circuit, ie $R_L = \infty$.

In this case $i_{C_1} = I$ is constant and the instantaneous power dissipation in Q_1 will depend on the instantaneous value of v_o. The maximum power dissipation will occur when $v_o = -V_{CC}$, for in this case v_{CE_1} is a maximum of $2V_{CC}$ and $P_{D_1} = 2V_{CC}I$. Observe that with an open-circuit load the average power dissipation in Q_1 is $V_{CC}I$

A far more dangerous situation occurs at the other extreme of R_L - specifically, $R_L = 0$. In the event of an output short circuit, a +ve i/p vg would theoretically result in an infinite load current. In practice a very large current may flow through Q_1 and if the short circuit condition

persists the resulting large power dissipation in Q_1 can raise its junction temperature beyond the specified maximum causing Q_1 to burn-up. To guard against such a situation, output stages are usually equipped with short circuit protection.

The power dissipation in Q_2 must be also taken into account in designing an emitter follower output stage. Since Q_2 conducts a constant current I, and the maximum value of v_{CE_2} is $2V_{CC}$ the maximum instantaneous power dissipation in Q_2 is $2V_{CC}I$. This maximum, however occurs when $v_o = V_{CC}$ a condition that would not normally prevail for a prolonged period of time.

12.2.4 Power Conversion Efficiency —

The power conversion efficiency of an output stage is defined as

$$\eta = \frac{\text{Load Power } (P_L)}{\text{Supply Power } (P_s)} \quad \text{—(1)}$$

For the emitter follower of fig (1), assuming that the output voltage is a sinusoid with the peak value $\hat{V}_o$, the average load power will be

$$P_L = \frac{(\hat{V}_o/\sqrt{2})^2}{R_L} = \frac{1}{2}\frac{\hat{V}_o^2}{R_L} \quad \text{—(2)}$$

Since the current in Q_1 is constant (I) the power drawn from the negative supply is $V_{CC}I$. The average current in Q_1 is equal to I and thus the average power drawn from the positive supply is $V_{CC}I$. Thus the total average supply power is

$$P_s = 2V_{CC}I \quad \text{—(3)}$$

$$\therefore \eta = \frac{1}{4}\frac{\hat{V}_o^2}{I R_L V_{CC}}$$

$$= \left(\frac{1}{4}\right)\left(\frac{\hat{V}_o}{I R_L}\right)\left(\frac{\hat{V}_o}{V_{CC}}\right) \quad \text{—(4)}$$

Since $\hat{V}_o \le V_{CC}$ & $\hat{V}_o \le I R_L$ maximum efficiency is obtained when

$$\hat{V}_o = V_{CC} = I R_L \quad \text{—(5)}$$

The max efficiency attainable is 25%

(41)

Because this is very low figure, the class A output stage is rarely used in high-power applications (>1W)

12.2.5 Transformer Coupled Power Amplifier

The transformer-less power amplifiers studied in previous section are called RC-coupled power amplifiers. We noted that the efficiency of RC coupled amplifiers is very poor. For ex, in case of a class-A power amplifier efficiency in the ideal case is just 25%.

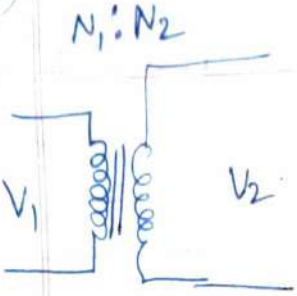
To improve efficiency, the transformer coupled class-A power amplifier is preferred. In these amplifiers a transformer is used to couple ac power to the load. By adjusting the turns ratio of the primary windings to the secondary windings, one can match the source and load impedance for maximum power transfer. This makes transformer-coupled power amplifiers more efficient as compared to RC-coupled power amplifiers, as maximum power transfer can take place.

The impedance matching of the transformer can be explained as follows-

$$\frac{V_1}{V_2} = \frac{N_1}{N_2} \quad \text{and} \quad \frac{I_1}{I_2} = \frac{N_2}{N_1} \quad \text{---(1)}$$

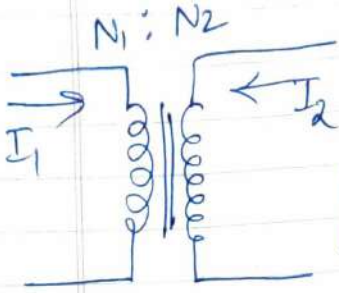
where N_1 (N_2), V_1 (V_2) and I_1 (I_2) are the number of turns, voltages and currents respectively, in the primary (secondary) coil of the transformer

(43)



$$\frac{V_2}{V_1} = \frac{N_2}{N_1}$$

fig (a)



$$\frac{I_2}{I_1} = \frac{N_1}{N_2}$$

fig (b)

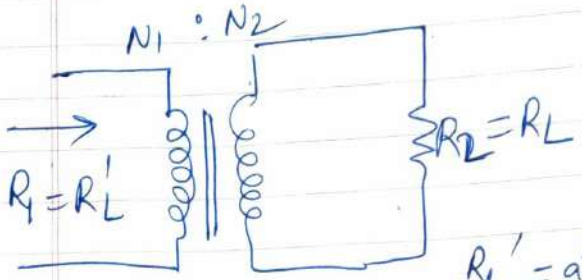


fig (c)

$$R_L' = a^2 R_L = \left(\frac{N_1}{N_2}\right)^2 R_L$$

('a' is turns ratio N_1/N_2)

Impedance Transformation

Boyle

Since the voltage and current can be changed by a transformer, an impedance "seen" from either side (primary or secondary) can also be changed.

As shown in fig (c) an impedance R_L is connected across the transformer secondary. The impedance is changed by the transformer when viewed at the primary side (R_L'). This can be shown as follows:

$$\frac{R_L}{R_L'} = \frac{R_2}{R_1} = \frac{V_2/I_2}{V_1/I_1} = \frac{V_2 I_1}{I_2 \cdot V_1} = \frac{V_2}{V_1} \cdot \frac{I_1}{I_2}$$

ie $\frac{R_L}{R_L'} = \frac{N_2}{N_1} \cdot \frac{N_2}{N_1}$

$\therefore R_L = \left(\frac{N_2}{N_1}\right)^2 R_L'$ ——— (2)

we can express the load resistance reflected to the primary side as -

or $R_L' = \left(\frac{N_1}{N_2}\right)^2 \cdot R_L$ ——— (3)

where R_L' is the reflected impedance or the effective load resistance.

From eqn (3) it can be noted that, the reflected impedace is related to the square of the turns ratio. If the number of turns of the secondary is smaller than that of the primary the impedance seen looking into the primary is larger than that of the secondary by the square of the turns ratio.

The schematic diagram of a transformer-coupled class-A power amplifier is shown in fig (d) below.

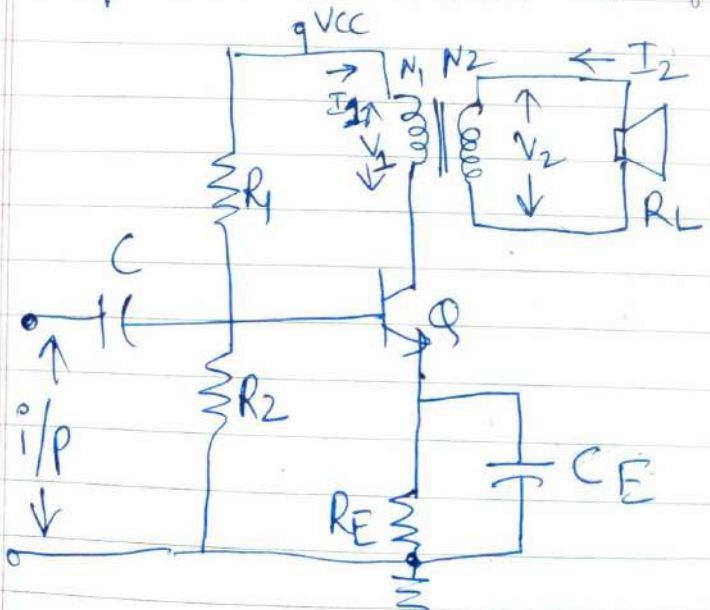


fig (d).

(4.5) The resistors R_1 and R_2 are used to bias the transistor for Class-A operation.

The dc and ac load lines for the amplifier are shown in fig (e)

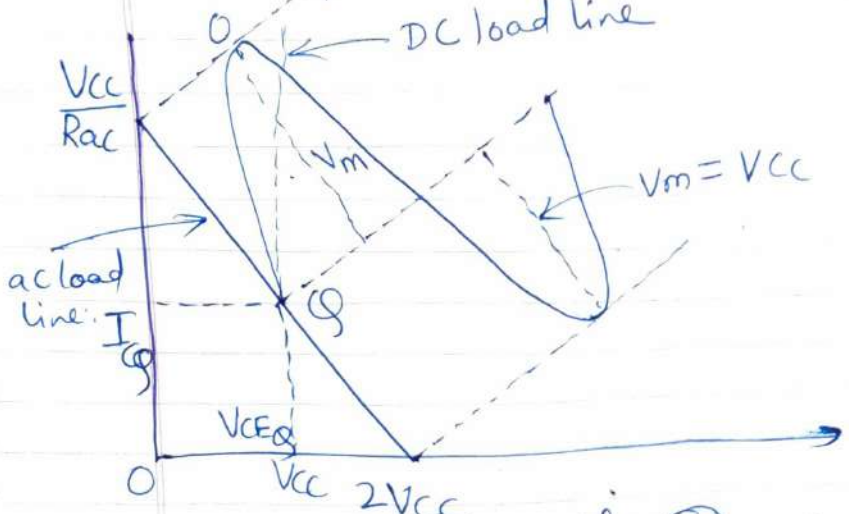


fig (e).

The load lines are drawn for ideal conditions i.e by assuming the dc resistance of the primary windings of the transformer to be zero. The dc load line is vertical at Vcc, with infinite slope, while the slope of the ac load line is $-(1/R_{ac})$ where R_{ac} is the ac resistance of the primary windings.

The interaction of the dc and the ac load lines gives the operating point of the amplifier. Due to the counter emf effect of the transformer, the output signal will swing from 0 to 2Vcc as shown in fig (e).

(46)

The efficiency of the power amplifier (η) is given by

$$\eta = \frac{\text{ac power delivered to the load}}{\text{dc power supplied}}$$

$$= \frac{P_{ac}}{P_{dc}}$$

DC power supplied is $= V_{CC} \cdot I_{CQ}$.

AC o/p power $P_{ac} = V_{rms} \cdot I_{rms}$

$$= \frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}$$

$$\therefore \eta = \frac{P_{ac}}{P_{dc}} = \frac{(V_{CC}/\sqrt{2})(I_{CQ}/\sqrt{2})}{V_{CC} I_{CQ}} \times 100$$

$$= \frac{1}{2} \times 100\ \%$$

$$= 50\%$$

Thus, in the ideal case, ie neglecting the power loss across the emitter bias resistor R_E and the dc resistance of the primary winding of the transformer, the efficiency of the transformer-coupled class-A amplifier is 50%, which is twice that of the RC coupled class-A power amplifiers.

Class A power amplifiers are used to supply power to transducers such as loud speaker in audio amplifier

Ex 12.1 A transformer-coupled class A power amplifier supplies power to an 80Ω load connected across the secondary of a step-down transformer having a turns ratio 5:1. Determine the maximum power output for a zero signal collector of 120mA.

Soln Load resistance $R_L = 80\Omega$.

Turns ratio $\alpha = 5 = \frac{N_1}{N_2}$

Load on the primary side of the transformer

$$R_L' = \left(\frac{N_1}{N_2}\right)^2 R_L$$

$$= 5^2 \cdot 80$$

$$= 2000\Omega$$

$I_C' = 120\,mA$

$I_{min} = 0\,mA$.

∴ RMS value of current

$$I_{rms} = \frac{1}{\sqrt{2}}\left[\frac{I_{max} - I_{min}}{2}\right]$$

$$= \frac{1}{2\sqrt{2}} \cdot 2I_C$$

$$= \frac{I_C}{\sqrt{2}}$$

Maximum power output

$$P_{out(max)} = I_{rms}^2 \cdot R_L'$$

$$= \frac{I_C'}{\sqrt{2}} \times R_L' = \frac{120\times10^{-3}}{2} \times 2000 = 14.4\,W$$

12.2.6 Class B Transformer-Coupled Amp^r

In the class B amplifier, the operating point is located in the cut-off region, hence the transistor conducts only for 180° or half of the input signal, making the Class B amplifier more efficient as compared to the class A amplifier.

In order to get the output signal for the complete cycle of the input signal two transistors are connected in push-pull configuration as shown in fig (a) below.

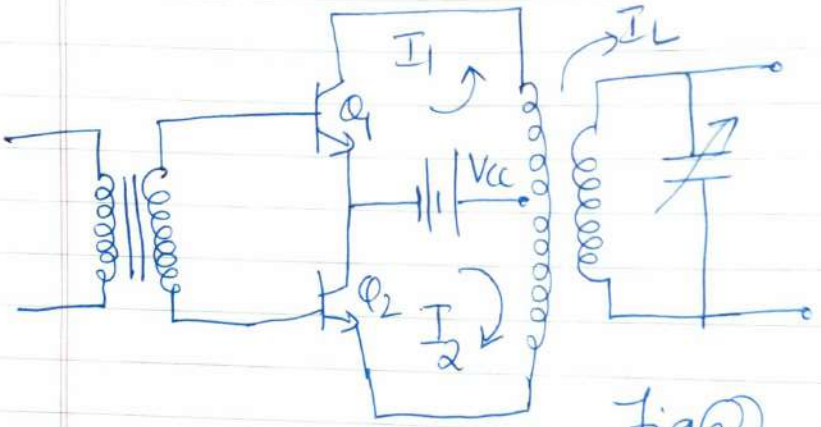


fig (a)

The class-B amplifier is used in RF transmitter circuits.

The transistors are biased such that in the absence of the RF signal, both transistors remain in the cut-off region and conduct no current. Fig (b) shows the current flowing through the dc power supply, each transistor and the load.

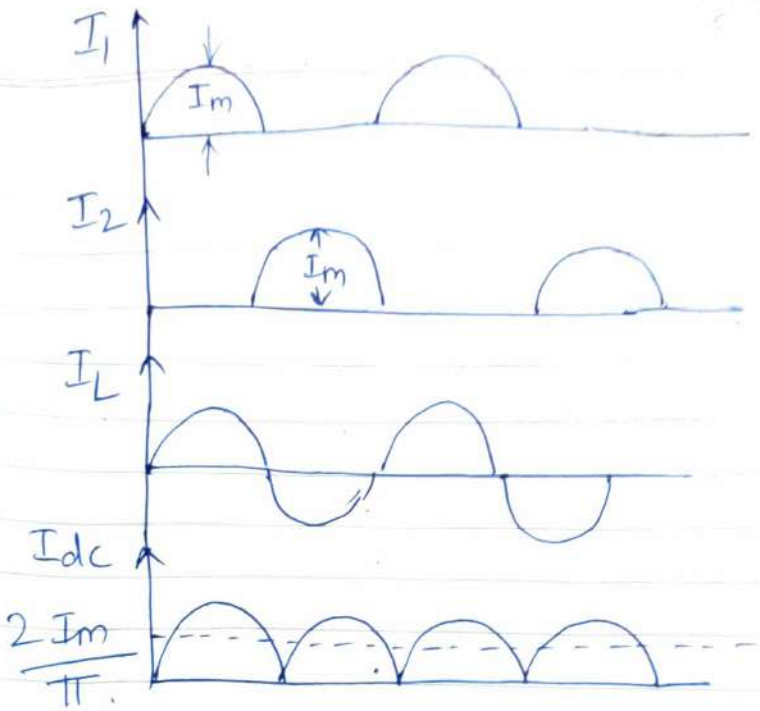


Fig (b)

The efficiency η of the amplifier is given by the ratio of the power delivered to the load to the dc power supplied.

AC power across the load is given by

$$P_{ac} = V_{rms} \cdot I_{rms} = \frac{V_{cc}}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}} = \frac{V_m \cdot I_m}{2}$$

As shown in fig (b), the current supply is like rectified full-wave pulses. Hence dc power dissipation is given by

$$P_{dc} = I_{dc} V_{cc}$$

$$= \frac{2I_m}{\pi} \times V_{cc}$$

$$= \frac{2 I_m V_m}{\pi}$$

Hence efficiency η is given by

$$\eta = \frac{\frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}}{\frac{2 I_m \cdot V_m}{\pi}} \times 100 = \frac{\pi}{4} \times 100 = 78.5\%$$

Thus the efficiency of the class-B amplifier is more than 78% which makes it useful for RF transmitters.

Ex 12.2 A class-B push-pull amplifier is supplied with $V_{cc} = 50V$. The signal brings the collector voltage down to $V_{min} = 5V$. The total dissipation from both transistors is 40W. Find the total power and conversion efficiency.

Solⁿ

$V_{cc} = 50V$

$V_{min} = 5V$

$P_d = 40W$

$P_d = P_{in(dc)} - P_{out(ac)}$

$$40 = \frac{2}{\pi} V_{cc} \cdot I_m - \frac{I_{cmax}(V_{cc} - V_{cmin})}{2}$$

$$I_m = \frac{40}{9.33}$$

$$= 4.287A$$

Total power input

$$P_{in(dc)} = \frac{2}{\pi} V_{cc} I_m$$

$$= \frac{2}{\pi} \times 50 \times 4.287$$

$$= 136.45W$$

(51)

$$P_{out(ac)} = \frac{I_m}{2}(V_{CC} - V_{Cmin})$$

$$= \frac{4.287}{2}(50-5)$$

$$= 99.65W \quad [\text{my ans } 96.4575]$$

$$\eta = \frac{P_{out(ac)}}{P_{in(dc)}} \times 100$$

$$= 73.03\%$$

12.3 Class-B Output Stage

Following fig ① shows a class-B output stage. It consists of a complementary pair of transistors (an npn and a pnp) connected in such a way that both cannot conduct simultaneously.

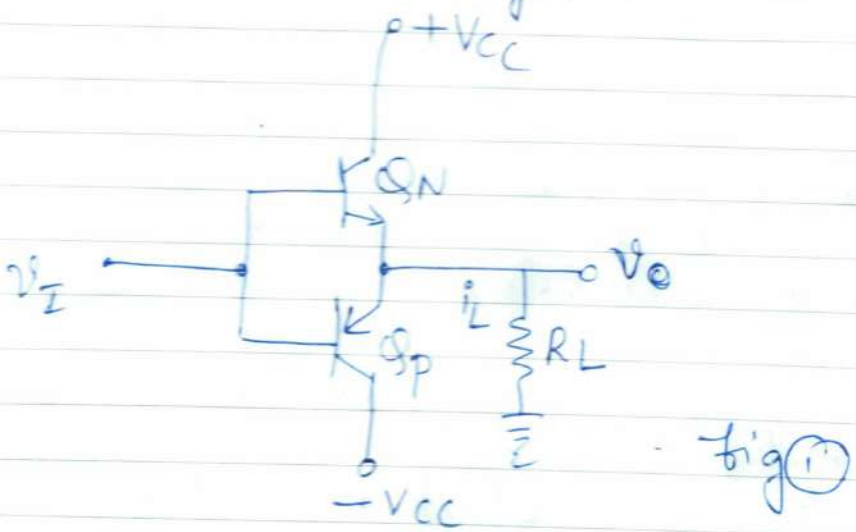


fig ①

When the input voltage v_I is zero, both transistors are cut-off and the output voltage v_o is zero.

As v_I goes positive and exceeds about 0.5V, Q_N conducts and operates as an emitter follower. In this case v_o follows v_I

ie $v_o = v_I - v_{BEN}$

and Q_N supplies the load current. Meanwhile the emitter-base junction of Q_p will be reverse biased by the V_{BE} of Q_N, which is approximately 0.7V. Thus Q_p will be cut-off

If the input goes negative by more than about 0.5V, Q_p turns on and acts as an emitter follower. Again v_o follows v_I

ie $v_o = v_I + v_{BEP}$

but in this case Q_p supplies the load current and Q_N will be cut-off

We conclude that the transistors in the class-B stage are biased at zero current and conduct only when the input signal is present.

The ckt operates in a 'Push-Pull' fashion. Q_N pushes (sources) current into the load when v_I is positive and Q_p pulls (sinks) current from the load when v_I is negative.

12.3.2 Transfer Characteristic

A sketch of the transfer characteristic of the class B stage is shown in Fig (2) below.

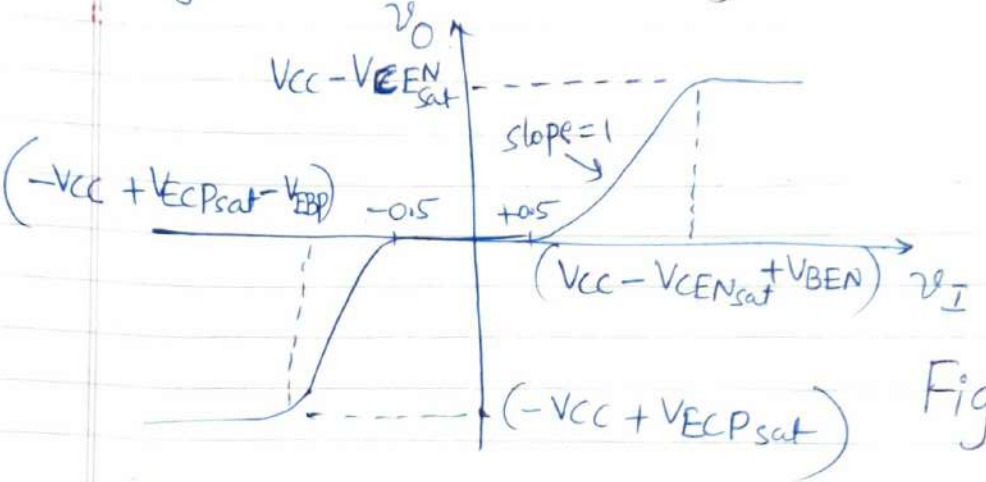


Fig (2)

Note that there exists a range of v_I centered around zero where both transistors are cut off and v_O is zero. This 'dead band' results in 'crossover distortion'

The effect of crossover distortion will be most pronounced when the amplitude of the input signal is small.

12.3.3 Power Conversion Efficiency

In order to calculate the power conversion efficiency η of the class-B stage, the crossover distortion is neglected and consider the case of an output sinusoid of peak amplitude $\hat{V}_o$. The average load power will be $P_L = \frac{1}{2}\frac{\hat{V}_o^2}{R_L}$ ——— (1)

The current drawn from each supply will consist of half sine waves of peak amplitude $(\hat{V}_o/R_L)$. Thus the average current drawn from each of the two power supplies will be $(\hat{V}_o/\pi R_L)$. It follows that the average power drawn from each of the two power supplies will be the same,

$$P_{S+} = P_{S-} = \frac{1}{\pi}\frac{\hat{V}_o}{R_L} V_{CC} \quad \text{——} (2)$$

and the total supply power will be

$$P_S = \frac{2}{\pi}\frac{\hat{V}_o}{R_L} V_{CC} \quad \text{——} (3)$$

Thus the efficiency will be given by

$$\eta = \left(\frac{1}{2}\frac{\hat{V}_o^2}{R_L}\right) \Big/ \left(\frac{2}{\pi}\frac{\hat{V}_o}{R_L} V_{CC}\right)$$

$$= \frac{\pi}{4}\frac{\hat{V}_o}{V_{CC}} \quad \text{——} (4)$$

It follows that the maximum efficiency is obtained when $\hat{V}_o$ is at its maximum. This maximum is limited by the saturation of Q_N and Q_P to $V_{CC} - V_{CEsat} \cong V_{CC}$.

At this value of peak output voltage, the power conversion efficiency is

$$\eta_{max} = \frac{\pi}{4} = 78.5\% \quad \text{——} (5)$$

This value is much larger than that obtained in the class A stage (25%)

Maximum average power available from class B output stage is obtained by substituting $\hat{V}_o = \frac{V_{CC}}{2}$ in eqn (1)

$$P_{L\,max} = \frac{1}{2}\frac{V_{CC}}{R_L} \quad \text{—— (6)}$$

12.3.4 Power Dissipation —

The quiscent power dissipation of the class B stage is zero. When an input signal is applied, the average power dissipated in the class B stage is given by

$$P_D = P_S - P_L \quad \text{—— (7)}$$

Substituting for P_S from eqn (3) and for P_L from eqn (1) results in

$$P_D = \frac{2}{\pi}\frac{\hat{V}_o}{R_L}V_{CC} - \frac{1}{2}\frac{\hat{V}_o^2}{R_L} \quad \text{—— (8)}$$

From symmetry, half of P_D is dissipated in Q_N and the other half in Q_P. Thus Q_N and Q_P must be capable of safely dissipating $\frac{1}{2}P_D$ Watts.

Since P_D depends on $\hat{V}_o$, the worst case of power dissipation must be found out.

Differentiating eqn (8) w.r.t $\hat{V}_o$, and equating the derivative

to zero gives the value of $\hat{V}_o$ that results in maximum average power dissipation as

$$\frac{dP_D}{d\hat{V}_o} = \frac{2V_{cc}}{\pi R_L} - \frac{1}{2R_L} 2\hat{V}_o = 0$$

$$\frac{\hat{V}_o}{R_L} = \frac{2V_{cc}}{\pi R_L}$$

ie $$\hat{V}_o\Big|_{P_{Dmax}} = \frac{2V_{cc}}{\pi} \quad \text{—— (9)}$$

Substituting this value in eq^n (8) we get

$$P_{Dmax} = \frac{2V_{cc}}{\pi R_L}\left(\frac{2V_{cc}}{\pi}\right) - \frac{1}{2R_L}\left(\frac{2V_{cc}}{\pi}\right)^2$$

$$= \frac{4V_{cc}^2}{\pi^2 R_L} - \frac{1}{2\pi^2 R_L} \cdot 4V_{cc}^2$$

$$= \frac{4V_{cc}^2}{\pi^2 R_L} - \frac{2V_{cc}^2}{\pi^2 R_L}$$

$$= \frac{2V_{cc}^2}{\pi^2 R_L} \quad \text{—— (10)}$$

Thus

$$P_{DNmax} = P_{DPmax} = \frac{V_{cc}^2}{\pi^2 R_L} \quad \text{— (11)}$$

(57)

At the point of maximum power dissipation the efficiency can be evaluated by substituting for $\hat{V}_o$ from eqn (9) into eqn (4) we get

$$\eta = \frac{\pi}{4}\left(\hat{V}_o / V_{cc}\right)$$

$$\eta = \frac{\pi}{4V_{cc}} \cdot \frac{2}{\pi} V_{cc}$$

$$= \frac{1}{2}$$

$$\eta\% = 50\%$$

Following fig (a) shows a sketch of P_D versus the peak output voltage $\hat{V}_o$

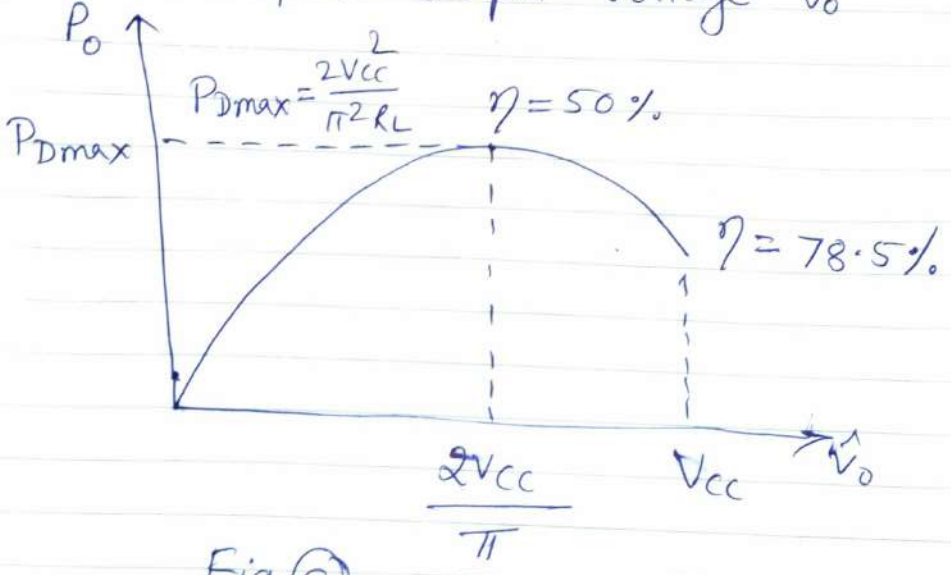
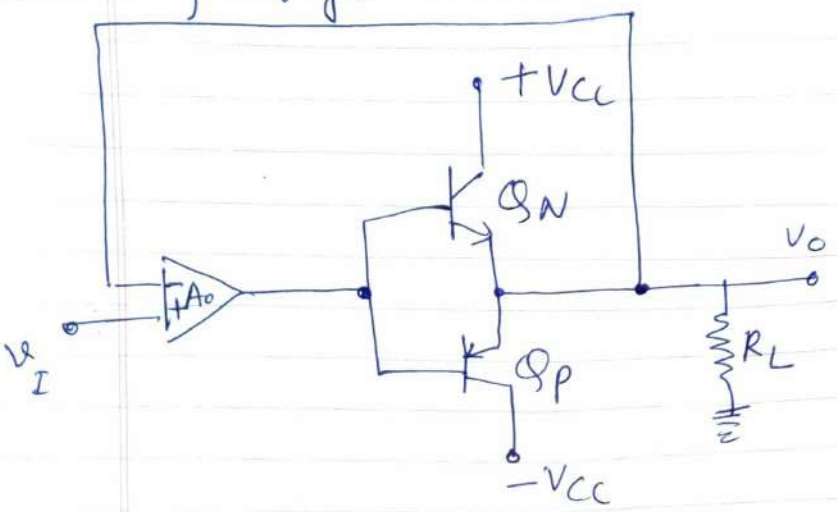


Fig (a).

It can be observed from above fig that increasing $\hat{V}_o$ beyond $2V_{cc}/\pi$ decreases the power dissipated in the class B stage, while increasing the load power. The price paid is an increase in nonlinear distortion as a result of approaching the saturation region of operation of Q_N and Q_P Transistor saturation flattens the peaks of the o/p sinewaveform

12.3.5 Reducing Crossover Distortion

The crossover distortion of a class-B output stage can be reduced substantially by employing a high gain op-amp and overall negative feedback as shown in the following fig.



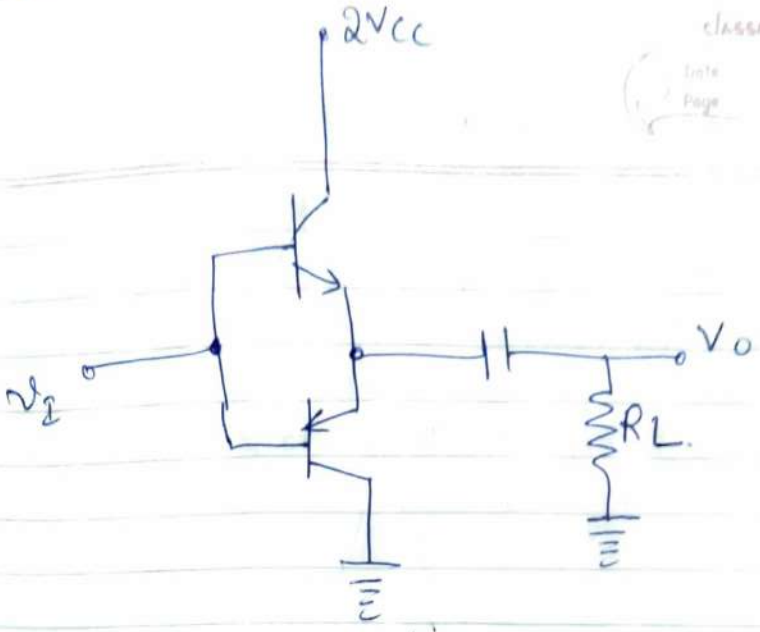
The ±0.7v deadband is reduced to ±0.7/Ao Volts, where Ao is the dc gain of the op-amp.

The disadvantage is that the slew rate of the op-amp will cause the alternate turning on and off of the output transistors to be noticeable espicially at high frequencies

12.3.6 Single-Supply Operation

The class-B stage can be operated from a single power supply, in which case the load is capacitively coupled as shown in the following fig.

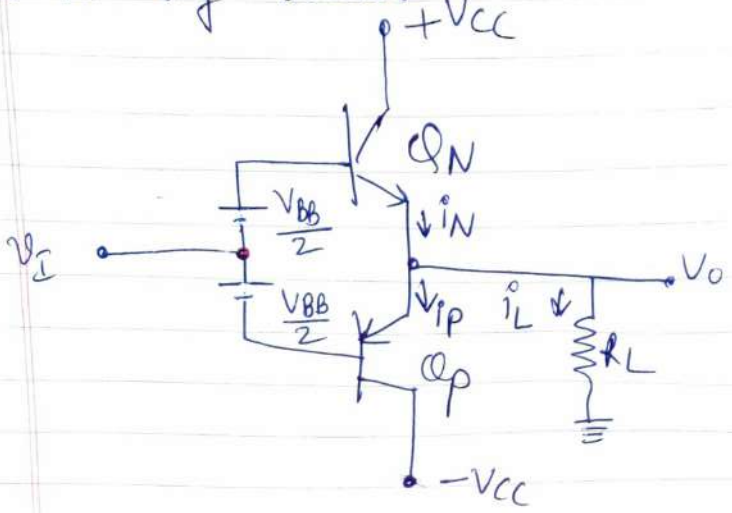
(59)



Note that in order to make the formulas derived in section 12.3.4 directly applicable, the supply voltage is denoted as 2Vcc.

12.4 Class AB Output Stage —

Crossover distortion can be eliminated by biasing the complementary output transistors at a small non-zero current. This results in the class AB output stage as shown in fig below.



The bias voltage V_{BB} is applied between the bases of Q_N and Q_p.

For $v_I = 0$, $v_o = 0$ and a voltage $V_{BB}/2$ appears across the base-emitter junction of each of Q_N and Q_p.

Assuming matched devices

$$i_N = i_p = I_Q = I_S e^{V_{BB}/2V_T} \quad \text{—(1)}$$

The value of V_{BB} is selected to yield the required quiescent current I_Q.

12.4.1 Circuit Operation —

When v_I goes positive by a certain amount, the voltage at the base of Q_N increases by the same amount and the output becomes positive at an almost equal value.

$$v_O = v_I + \frac{V_{BB}}{2} - v_{BEN} \quad \text{—— (2)}$$

The positive v_O causes a current i_L to flow through R_L and thus i_N must increase, that is

$$i_N = i_P + i_L \quad \text{—— (3)}$$

The increase in i_N will be accompanied by a corresponding increase in v_{BEN} (above the quicent value of $V_{BB}/2$). However, since the voltage between the two bases remains constant at V_{BB}, the increase in v_{BEN} will result in an equal decrease in v_{EBP} and hence in i_P.

The relationship between i_N and i_P can be derived as follows.

$$v_{BEN} + v_{EBP} = V_{BB}$$

$$V_T \ln \frac{i_N}{I_S} + V_T \ln \frac{i_P}{I_S} = 2V_T \ln \frac{I_Q}{I_S}$$

$$i_N i_P = I_Q^2 \quad \text{—— (4)}$$

Thus as i_N increases, i_P decreases by the same ratio while the product remains constant.

Equations (3) and (4) can be combined to yield i_N for a given i_L

as the solution to the quadratic equation

$$i_N^2 - i_L i_N - I_Q^2 = 0 \quad \text{---(5)}$$

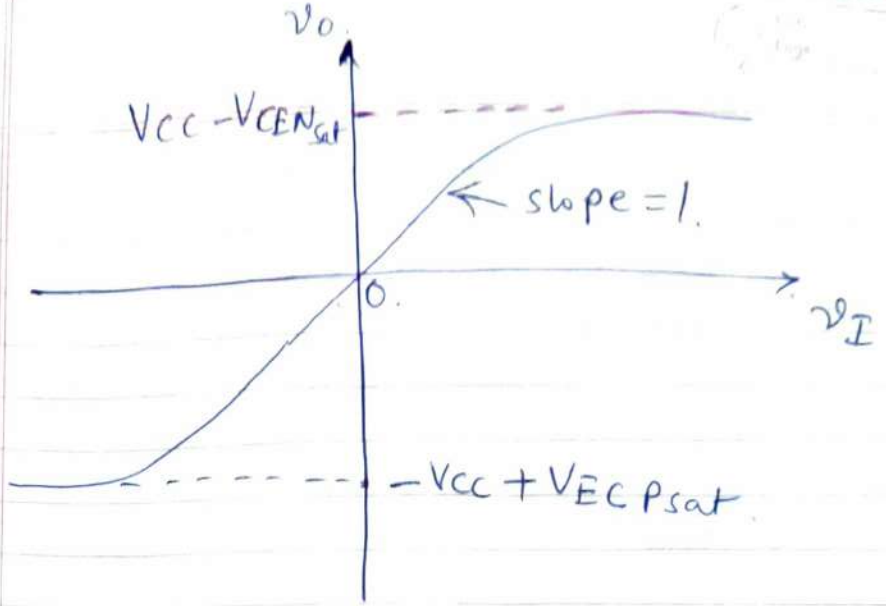
From the equations above, it can be observed that for positive output voltages, the load current is supplied by Q_N, which acts as the output emitter follower. Meanwhile, Q_P will be conducting a current that decreases as v_O increases; for large v_O the current in Q_P can be ignored totally.

For negative input voltages the opposite occurs. The load current is supplied by Q_P, which acts as the output emitter follower; while Q_N conducts a current that gets smaller as v_I becomes more negative. Eqn (4) relating i_N and i_P holds for -ve inputs as well.

We conclude that the class AB stage operates in the same manner as the class B circuit with the exception that, for small v_I both transistors conduct, and as v_I is increased & decreased one of the two transistors takes over the operation.

Since the transition is a smooth one the crossover distortion is almost totally eliminated. Following fig shows the transfer characteristic of the class AB stage.

(63)

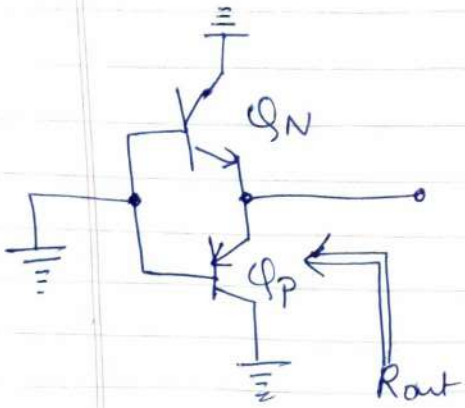


The power relationships in the class AB stage are almost identical to those derived for the class B ckt. The only difference is that under quicent conditions the class AB ckt dissipates a power of $V_{CC} I_Q$ per transistor. Since I_Q is usually much smaller than the peak load current, the quiscent power dissipation is usually small.

~~12.4.2 Output~~

12.4.2 Output Resistance

If we assume that the source supplying v_i is ideal, then the output resistance of the class AB stage can be determined from the ckt shown in the fig below.



$$R_{out} = r_{eN} \| r_{ep} \quad \text{—(1)}$$

where r_{eN} and r_{ep} are the small-signal emitter resistances of Q_N and Q_P respectively.

At a given input voltage, the currents i_N and i_p can be determined, and r_{eN} and r_{ep} are given by

$$r_{eN} = \frac{V_T}{i_N} \quad \text{—(2)}$$

$$r_{ep} = \frac{V_T}{i_P} \quad \text{—(3)}$$

Note: recall eqn's (19) (20) (21) of section 3.6.3

where V_T is a const called thermal voltage and is given by

$$V_T = \frac{kT}{q}$$

where k = Boltzmann's const

$= 1.38 \times 10^{-23}$ Joules/kelvin

T = The absolute temp in kelvins
= 273 + temp in °C

q = The magnitude of electronic charge
= 1.6×10^{-19} coulomb

For ckt analysis we use $V_T \cong 25$ mV at room temp.

Thus, $R_{out} = \frac{V_T}{i_N} \| \frac{V_T}{i_p}$

$$= \frac{V_T}{i_N + i_p} \quad \text{——— (4)}$$

Since as i_N increases, i_p decreases and vice versa, the output resistance remains approximately constant in the region around $V_I = 0$. This in effect is the reason for the virtual absence of crossover distortion.
At larger load currents either i_N or i_p will be significant and R_{out} decreases as the load current increases.

12.6 Class C Output Stage —

The class A power amplifier is biased in the active region to produce a linear output signal with minimal distortion. However due to this biasing arrangement, the transistor remains ON even for no input signal. This results in the poor efficiency of the class-A power amplifier. In order to improve efficiency, the class C power amplifier is used.

In the class C amplifier, the transistor is biased such that it remains OFF for no-signal conditions and operates in the saturation region when an input signal is present. When the transistor is OFF, the current through it is very small and hence the transistor dissipates negligible power. Similarly, when the transistor operates in saturation, the voltage across it is very small, and again the power dissipation is small. Therefore, in the class-C amplifier, as the transistor dissipates less power, its efficiency is higher than that of the class-A amplifier. However, the class-C amplifier is highly nonlinear and produces distorted output. This drawback of class C amplifier is overcome by connecting a low pass filter

at the output. The low pass filter blocks all high-frequency harmonics and passes only signal frequency to the load.

The schematic diagram of a class-C amplifier is shown in fig (a) below

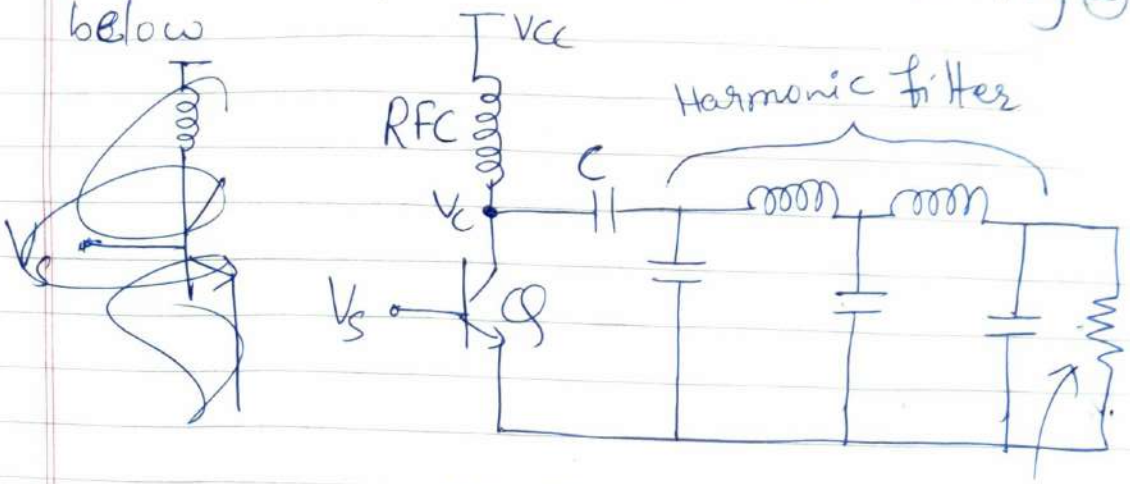
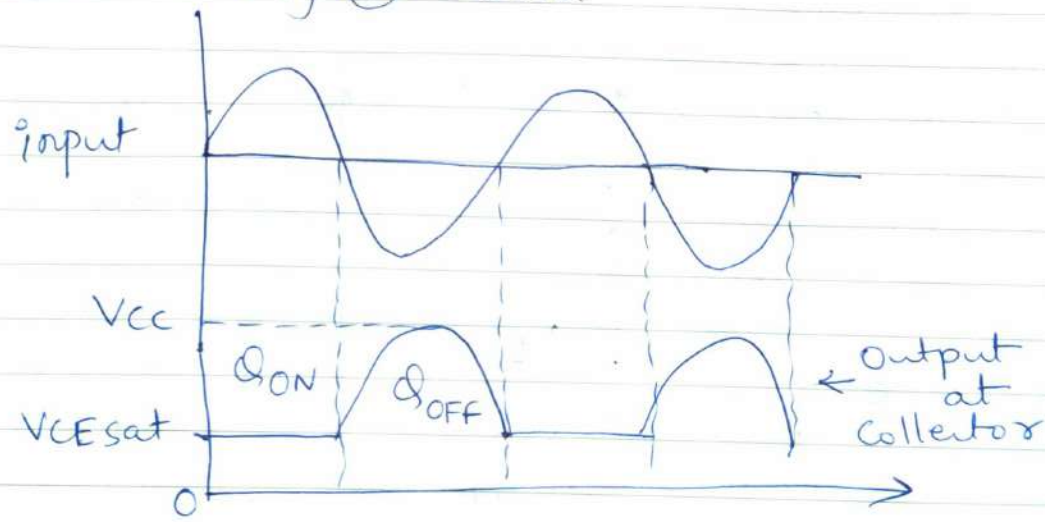


Fig (a)

The input and the waveforms at the collector terminal are shown in Fig (b) below.



When the input signal is positive and above the cut-in voltage of the transistor, the transistor operates in the saturation region. During this period the output voltage is

equal to the saturation voltage of the transistor. When the input voltage is less than the cut in voltage, the transistor remains off, while the induced emf in the inductor provides the collector voltage This output voltage is fed to the low pass filter as shown in fig (a) The low pass filter suppresses the high frequency harmonics present at the collector and produces output similar to the input signal.

12.6.1 Efficiency of Class C Amplifier

To derive an analytical expression for the power conversion efficiency, the class C amplifier is modelled as shown in the fig (a) below

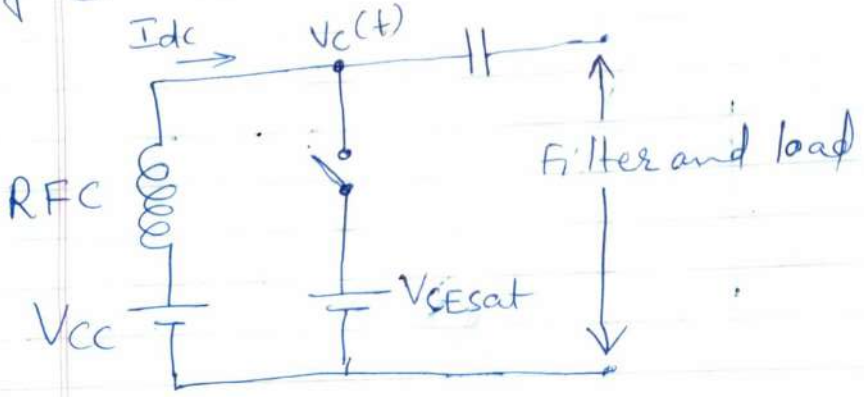


Fig (a)

The output waveforms is shown in Fig (b) below

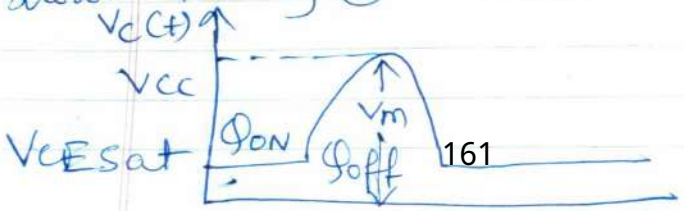


Fig (b).

According to the model shown in Fig(a), the collector voltage when transistor is OFF, ie the switch is open, is given by

$$V_c(t) = V_{CEsat} + V_m \cos(\omega t)$$

When the transistor is ON, ie the switch is closed is given by

$$V_c(t) = V_{CEsat}$$

However, in the class C amplifier, the time-average value of $V_c(t)$ must be zero, as the dc resistance of the coil used is approximately zero, hence we can write

$$\frac{1}{T}\int_0^T = V_{CC}$$

As V_{CEsat} is very small as compared to V_m, the above expression can be modified as follows:

$$V_{CC} = V_{CEsat} + \frac{1}{T}\int_0^{T/2} V_c(t)$$

$$= V_{CEsat} + \frac{1}{T}\int_0^{T/2} V_m(t)\cos(\omega t)\,dt$$

$$= V_{CEsat} + \frac{V_m}{\pi}$$

$$V_m = \pi (V_{CC} - V_{CEsat})$$

The dc power supplied is given by

$$P_{dc} = V_{CC} I_{dc}$$

(10)

The remaining power

where Idc is the average value of the supply current. Due to the blocking capacitor, the same average current flows through the transistor when it is in saturation.

The power dissipated by the transistor is given by

$$P_T = V_{CEsat} I_{dc}$$

The remaing power must appear as useful ac power across the load; hence the ac output power is given by

$$P_{ac} = P_{dc} - P_T$$
$$= V_{CC} I_{dc} - V_{CEsat} I_{dc}$$
$$= (V_{CC} - V_{CEsat}) I_{dc}$$

Hence the efficiency of the class C amplifier is given by

$$\eta = \frac{P_{ac}}{P_{dc}} = \frac{(V_{CC} - V_{CEsat}) I_{dc}}{V_{CC} I_{dc}}$$

$$= 1 - \frac{V_{CEsat}}{V_{CC}}$$

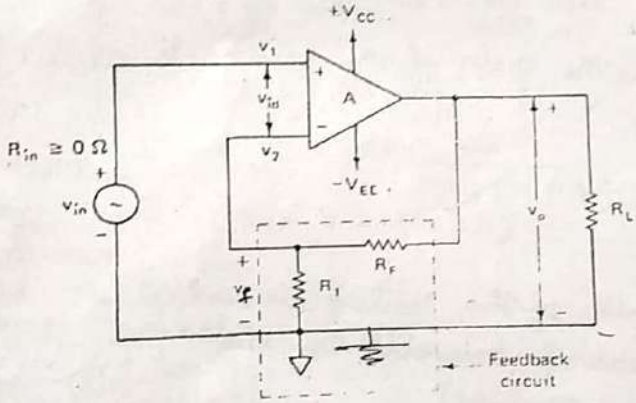
As V_{CEsat} is very small as compared to V_{CC}, the efficiency of the class C amplifier is very high; it can achieve above 90% efficiency.

2018 Scheme
MODULE 04

OP-Amp with Negative Feedback and General Applications

Voltage-Series feedback Amplifier

* The op-amp is represented by its schematic symbol, including its large-signal voltage gain A, and the feedback circuit is composed of two resistors, R_1 and R_F.
* The circuit is commonly know as a non inverting amplifier with feedback because it uses feedback, and the input signal is applied to the non inverting input terminal of the op-amp.
* Open-loop voltage gain (or gain without feedback) $A = \frac{V_o}{V_{id}}$
* closed loop voltage gain (or gain with feedback) $A_F = \frac{V_o}{V_{in}}$
* gain of the feedback circuit. $B = \frac{V_f}{V_o}$



Negative Feedback

* Referring to the above circuit
* Kirchoff's voltage equation for the input loop is

$V_{in} = V_1$, $V_f = V_2$ (3-1)

$V_{id} = V_1 - V_2$; $V_{id} = V_{in} - V_f$

where V_{in} = input voltage
V_f = feedback voltage
V_{id} = difference input voltage

* An op-amp always amplifies the difference input voltage V_{id}. From eq^n (3-1) this difference voltage is equal to the input voltage V_{in} minus the feedback voltage V_f. In other
* In other words, the feedback voltage always opposes the input voltage (or is out of phase by 180° with respect to the input voltage) hence the feedback is said to be negative.

Closed-loop voltage Gain

The closed-loop voltage gain is

$$A_F = \frac{V_o}{V_{in}}$$

WKT, $V_o = A(V_1 - V_2)$

By refering to the above figure

$V_1 = V_{in}$

$V_2 = V_f = \frac{R_1 V_o}{R_1 + R_F}$ Since $R_i \gg R_1$

$\therefore V_o = A\left(V_{in} - \frac{R_1 V_o}{R_1 + R_F}\right) \rightarrow (1)$

$$V_o = \frac{A(R_1 + R_F) V_{in}}{R_1 + R_F + AR_1}$$

$$A_F = \frac{V_o}{V_{in}} = \frac{A(R_1 + R_F)}{R_1 + R_F + AR_1}$$

generally, A is very large $AR_1 \gg (R_1 + R_F)$ and $(R_1 + R_F + AR_1) \cong AR_1$

$$A_F = \frac{V_o}{V_{in}} = 1 + \frac{R_F}{R_1}$$

from (1)

$$V_o = AV_{in} - \frac{AR_1 V_o}{R_1 + R_F}$$

$$V_o + \frac{AR_1 V_o}{R_1 + R_F} = AV_{in}$$

$$V_o\left(1 + \frac{AR_1}{R_1 + R_F}\right) = AV_{in}$$

$$V_o\left(\frac{R_1 + R_F + AR_1}{R_1 + R_F}\right) = AV_{in}$$

$$V_o = \frac{AV_{in}(R_1 + R_F)}{R_1 + R_F + AR_1}$$

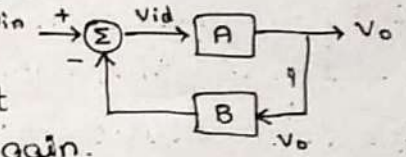
As defined previously, the gain of the feedback circuit (B) is the ratio of V_f and V_o

$$\therefore B = \frac{V_f}{V_o} = \frac{R_1}{R_1 + R_F}$$

$$A_F = \frac{1}{B}$$

~~{This means that the gain of the feedback and also indicates the relationship between the different variables of the system. The bl}~~

Block diagram representation of non-inverting amplifier with feedback.



* This means that the gain of the feedback circuit is the reciprocal of the closed loop voltage gain.
* In other words, for given R_1 and R_F the values of A_F and B are fixed.
* ~~Besides~~ Finally, the closed loop voltage gain A_F can be expressed in terms of open loop gain A and feedback circuit gain B as follows.

$$A_F = \frac{A\left(\frac{R_1 + R_F}{R_1 + R_F}\right)}{\frac{R_1 + R_F}{R_1 + R_F} + \frac{AR_1}{R_1 + R_F}}$$

$$A_F = \frac{A}{1 + AB}$$

where A_F = closed-loop voltage gain
A = open-loop voltage gain
B = gain of the feedback circuit
AB = loop gain

$$\frac{V_f}{V_o} = \frac{\frac{R_1 V_o}{R_1 + R_F}}{\frac{AV_{in}(R_1 + R_F)}{R_1 + R_F + AR_1}}$$

$$\frac{\frac{AV_o}{R_1 + R_F}}{\frac{A_F \cdot V_{in}}{V_o}}$$

...rence Input voltage Ideally zero

...t us reconsider $V_{id} = \frac{V_o}{A}$

Since A is very large (ideally infinite), $V_{id} \cong 0$

i.e., $V_1 \cong V_2 \rightarrow (1)$

$V_1 = V_{in}$

$V_2 = V_f$

$V_2 = \frac{R_1 V_o}{R_1 + R_F}$

Substituting these values of V_1 and V_2 in (1)

$$V_{in} = \frac{R_1 V_o}{R_1 + R_F}$$

$$A_F = \frac{V_o}{V_{in}} = 1 + \frac{R_F}{R_1}$$

Input Resistance with Feedback (Open loop)

In this circuit R_i is the input resistance of the op-amp and R_{iF} is the input resistance ~~resistance~~ of the amplifier with feedback The input resistance with feedback is defined as

$$R_{iF} = \frac{V_{in}}{i_{in}}$$

$$R_{iF} = \frac{V_{in}}{V_{id}/R_i}$$

$V_{id} = \frac{V_o}{A}$ and $V_o = \frac{A}{1+AB} V_{in}$

$$\therefore R_{iF} = R_i \frac{V_{in}}{V_o/A}$$

$$= AR_i \frac{V_{in}}{AV_{in}(1+AB)}$$

$$R_{iF} = R_i(1+AB)$$

This means that the input resistance of the op-amp with feedback is $(1+AB)$ times that without feedback.

fig (1)

~~Fig 3 + 1b~~

Output Resistance with feedback

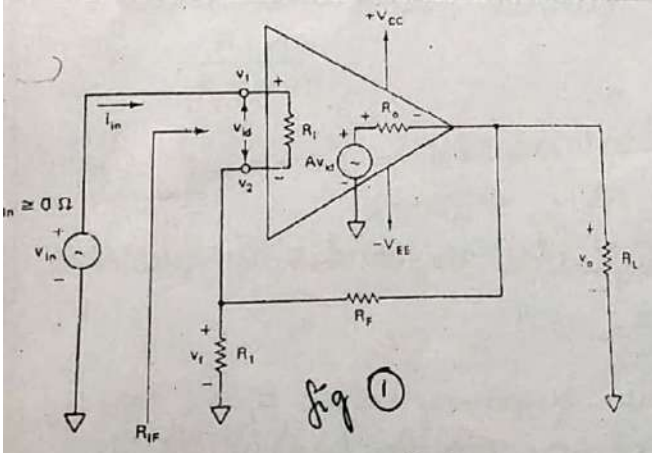


fig (1)

a Derivation of input resistance with feedback

output resistance is the resistance determined looking back into the v -back amplifier from the output terminal as shown in Figure. Thus, resistance can be obtained by using Thevenin's theorem for dependent sources.

Specifically to find output resistance with feedback R_{OF} reduce independent source V_{in} to zero, apply an external voltage V_o and then calculate the resulting current i_o.

$$R_{OF} = \frac{V_o}{i_o} \rightarrow (1)$$

writing Kirchhoff's current equation at output node N, we get

$$i_o = i_a + i_b$$

Since $[(R_F + R_1) \| R_i] \gg R_o$ and $i_d \gg i_b$ $\therefore i_o \cong i_a$

The current i_o can be found by writing Kirchhoff's voltage equation for the output loop

$$V_o - R_o i_o - AV_{id} = 0$$

$$i_o = \frac{V_o - AV_{id}}{R_o}$$

however, $V_{id} = V_1 - V_2$

$$= 0 - V_2$$

$$= -\frac{R_1 V_o}{R_1 + R_F} = -BV_o$$

fig (2)

$$i_o = \frac{V_o + ABV_o}{R_o}$$

Substituting the value of i_o in (1) $R_{OF} = \frac{V_o}{(V_o + ABV_o)/R_o} = \frac{V_o R_o}{V_o + ABV_o} = \frac{V_o R_o}{V_o(1+AB)}$

$$\therefore R_{OF} = \frac{R_o}{1+AB}$$

This result shows that the output resistance of the voltage series feedback amplifier is $\left(\frac{1}{1+AB}\right)$ times the output resistance R_o of the op-amp. That is, the output resistance of the op-amp with feedback is much smaller than the output resistance without feedback

Bandwidth with Feedback

The Bandwidth of an amplifier is defined as the band of frequencies for which the gain remains constant.

Fig shows the open loop gain versus frequency curve of the 741 C op-amp. From this curve for a gain of 200,000 the bandwidth is approximately 5Hz or the gain of (200,000 × 5Hz) = 1MHz

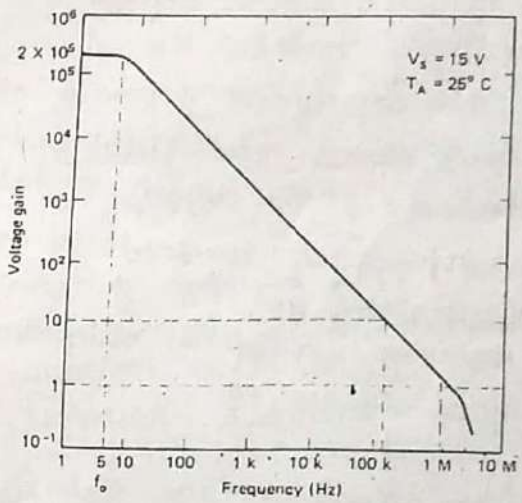
Bandwidth Product

the other extreme, the bandwidth is approximately 1MHz when the gain 1.

* Thus, the gain-bandwidth product is constant.
* However, this ~~of~~ holds true only for op-amps like the 741 that have just one break frequency below unity gain bandwidth.
* For the 741, 5Hz is the break frequency; the frequency at which the gain A is 3dB down from its value at 0Hz. ~~we~~ -
* we will denote it by f_o. on the other hand, the frequency at which the gain equals 1 is known as the unity gain bandwith.
* The relationship between the break frequency f_o, open loop voltage gain A, bandwidth with feedback f_F, and the closed loop gain A_F can be established as follows.
* Since for an op-amp with a single break frequency f_o the gain-bandwidth product is constant and equal to the unity gain-bandwidth

$$UGB = (A)(f_o)$$

where A = open-loop voltage gain
f_o = break frequency of an op-amp



$$UGB = (A_F)(f_F)$$

where A_F = closed-loop voltage gain
f_F = bandwith with feedback

∴ equating both equation

$$(A)(f_o) = (A_F)(f_F)$$

$$f_F = \frac{A f_o}{A_F}$$

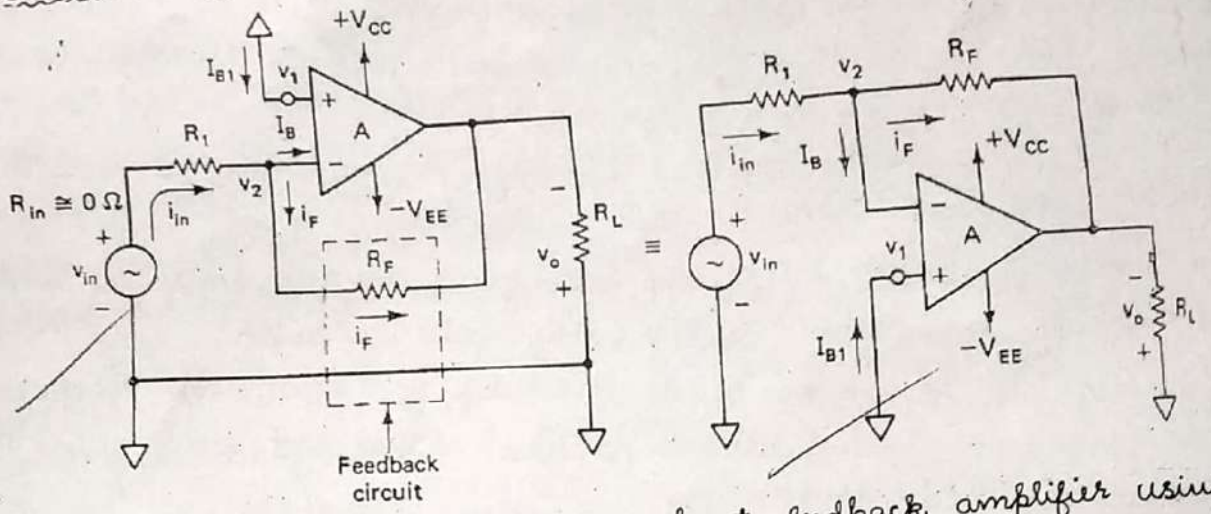
for non inverting amplifier with feedback

$$A_F = \frac{A}{1 + AB}$$

$$f_F = \frac{A f_o}{A/(1+AB)}$$

$f_F = f_o(1 + AB)$ → indicates that the bandwidth of the non-inverting amplifier with feedback f_F is equal to its bandwidth without feedback, f_o times $(1+AB)$.

Voltage Shunt Feedback Amplifier



★ The above figure shows the voltage shunt feedback amplifier using an op-amp.

★ The input voltage drives the inverting terminal, and the amplified as well as inverted output signal is also applied to the inverting input via the feedback resistor R_F

★ This arrangement forms a negative feedback because any increase in the output signal result in a feedback signal into the inverting input causing a decrease in the output signal.

★ Non inverting terminal is grounded and the feedback circuit has only one resistor RF.

★ However, an extra resistor R_1 is connected in series with the input signal source Vin.

Closed-loop voltage Gain

The closed-loop voltage gain A_F of the voltage-shunt feedback amplifier can be obtained by writing Kirchhoff's current equation at the input node V_2.

$$i_{in} = i_F + I_B$$

Since R_i is very large, the input bias current I_B is negligibly small. For instance $R_i = 2M\Omega$ and $I_B = 0.5\mu A$ for the 741C

$$\therefore i_{in} \cong i_F$$

$$\frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_o}{R_F} \rightarrow (1)$$

$$V_1 - V_2 = \frac{V_o}{A} \quad \text{wkt} \quad A = \frac{V_o}{V_{id}} \; ; \; V_{id} = V_1 - V_2$$

$V_1 = 0V$

$$V_2 = -\frac{V_o}{A} \; ; \text{ Sub in } (1)$$

$$\frac{V_{in} + V_o/A}{R_1} = -\frac{(V_o/A) - V_o}{R_F}$$

$$A_F = \frac{V_o}{V_{in}} = -\frac{ARF}{R_1 + RF + AR_1}$$

$$\frac{AV_{in} + V_o}{AR_1} = \frac{-V_o - V_oA}{R_F A}$$

$$R_F AV_{in} + R_F V_o = -V_o R_1 - V_o AR_1$$

$$R_F AV_{in} = -V_o R_1 - V_o AR_1 - R_F V_o$$

$$-ARF = \frac{V_o}{V_{in}}(R_1 + AR_1 + R_F)$$

negative sign indicates that the input and output signals are out phase by 180°.

In fact, because of this phase inversion the configuration is commonly called an inverting amplifier with feedback.

* Since the internal gain A of the op-amp is very large $AR_1 \gg R_1 + R_F$.

$$A_F = \frac{V_o}{V_{in}} = -\frac{R_F}{R_1} \quad \text{(ideal)} \quad \rightarrow ①$$

* This equation shows that the gain of the inverting amplifier is set by selecting a ratio of feedback resistance R_F to the input resistance R_1.
* In fact, the ratio R_F/R_1 can be set to any value whatsoever, even to less than 1.
* Because of this property of the gain equation, the inverting amplifier configuration with feedback lends it self to a majority of applications as against those of the non inverting amplifier.
* It facilitates analysis of the inverting amplifier with feedback.
* It helps compare and contrast inverting and non inverting amplifier configurations.

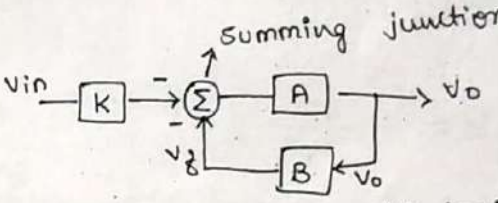
÷ num & deno by $R_1 + R_2$ eqn ①

$$A_F = \frac{-A(R_F/R_1 + R_F)}{1 + \frac{AR_1}{R_1 + R_F}} = -\frac{AK}{1+AB}$$

$$\therefore A_F = \frac{-AK}{1+AB}$$

* where $K = \frac{R_F}{R_1 + R_F}$, a voltage attenuation factor

$B = \frac{R_1}{R_1 + R_F}$, gain of the feedback circuit.



inverting amplifier with feedback using a voltage summing junction as a model for current summing.

If $AB \gg 1$, then $(1+AB) \cong AB$

$$\therefore A_F = -\frac{K}{B}$$

$$A_F = -\frac{R_F}{R_1}$$

Inverting input terminal at virtual Ground

* Refering above voltage shunt feedback amplifier.
* Non inverting terminal is grounded. and the input signal is applied to the inverting terminal via resistor R_1.
* However, as discussed in section Difference input voltage ideally zero. that is the voltage at the inverting terminal (V_2) is approxi-mately equal to the non inverting terminal (V_1).

* In other words, the inverting terminal voltage V_2 is approximately ground potential.
* ∴ the inverting terminal is said to be at virtual ground.
* This concept is extreamly useful in the analysis of closed-loop inverting amplifier circuits

$$i_{in} \cong i_F$$

$$\frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_o}{R_F}$$

$$V_1 = V_2 \pm 0V$$

$$\frac{V_{in}}{R_1} = -\frac{V_o}{R_F}$$

$$A_F = \frac{V_o}{V_{in}} = -\frac{R_F}{R_1}$$

Input Resistance with Feedback

* The easiest method of finding the input resistance is to millerize the feedback resistor R_F ; that is split R_F into its two Miller components

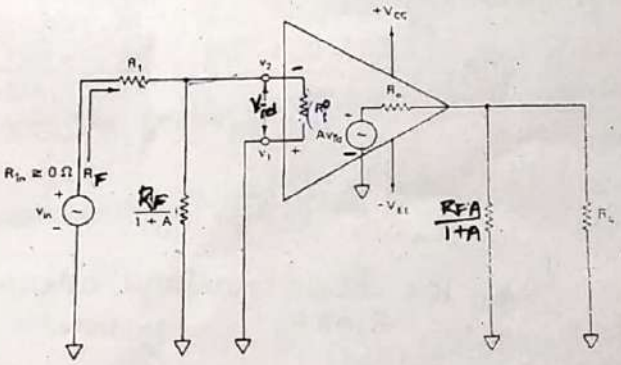
$$R_{iF} = R_1 + \frac{R_F}{1+A} \parallel R_i$$

Since R_i and A are very large

$$\frac{R_F}{1+A} \parallel R_i \cong 0\,\Omega$$

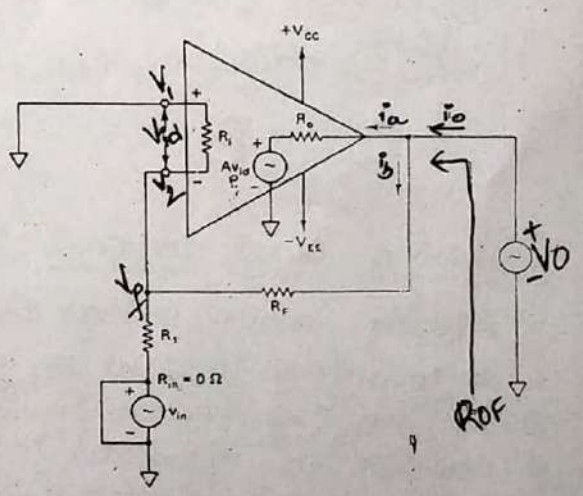
$R_{iF} \cong R_1$ (Ideal)

$R_{iF} = R_1$ —11—



Output Resistance with Feedback

* The o/p resistance with feedback R_{OF} is the resistance measured at the output terminal of the feedback amplifier.
* The o/p resistance of the noninverting amplifier was obtained by Thevenin's theorem we can do the same for the inverting amplifier.
* Thevenin's equivalent circuit is exactly the same as that for the non inverting amplifier. because the output resistance R_{OF} of the inverting amplifier must be identical to that of the noninverting amplifier



$$R_{OF} = \frac{R_O}{1+AB}$$

where R_O = output resistance of the op-amp
A = open-loop voltage gain of the op-amp
B = gain of the feedback circuit.

Bandwidth with Feedback

* The gain-bandwidth product of a single break frequency op-amp is always constant.
* We also saw that the gain of the amplifier with feedback is always less than the gain without feedback.
* Bandwidth of the amplifier with feedback f_F must be larger than that without feedback

$$f_F = f_o(1+AB)$$

where f_o = break frequency of the op-amp

$$f_o = \frac{\text{unity gain bandwidth}}{\text{open-loop voltage gain}}$$

$$f_o = \frac{UGB}{A}$$

$$f_F = \frac{UGB}{A}(1+AB)$$

$$f_F = \frac{(UGB)(K)}{A_F}$$

$$A_F = -\frac{AK}{1+AB}$$

$$\frac{A_F}{K} = -\frac{A}{1+AB}$$

where $K = \frac{R_F}{R_1+R_F}$ $\quad A_F = \frac{AK}{1+AB}$

* To find the closed-loop bandwidth of the inverting amplifier if f_o is known & if unity gain-bandwidth (UGB) is given.
* However, to calculate the bandwidth graphically from the gain versus frequency curve.
* It is obvious that for the same closed loop gain the closed-loop bandwidth for the inverting amplifier is lower than that for the non inverting amplifier by a factor of $K (<1)$, if $A_F = 1$

$f_F = UGB$ for the non inverting amplifier

$f_F = \frac{UGB}{2}$ for the inverting amplifier, since $R_1 = R_F$

* As closed loop gain A_F approaches the open-loop gain A, the difference between the non-inverting and inverting amplifier bandwidths approches zero.
* As an extreme limit when $K \cong 1$ the value of f_F for both the non inverting & inverting approximately the same

DC Amplifier :-

* Basically an op-amp can amplify two types of signals : dc and ac.
* In a dc amplifier the output signal changes in response to chang in its dc input levels.
* A dc amplifier can be inverting, non inverting, or differential as sho in the figures. ① & ②
* To reduce the output offset voltage to zero. that is to improve the accuracy of the dc amplifier. the offset null circuitry of the op-amp should be used.
* For op-amps without offset null capability the external offset voltage compensating network should be used.
* otherwise, a high-precision op-amp such as the μA 714 which has smaller offsets and drifts must be used.

AC Amplifier :-

However if the designer needs the ac response characteristics of the op-amp that is low and high frequency limits. or if the ac input is riding on some dc level it is necessary to use an ac amplifier with coupling capacitor.

For example in an audio receiver system that consists of a number of stages because of thermal drift, component tolerances and variations the dc level is produced. To prevent the amplification of such dc levels coupling capacitors must be used between the stages.

The coupling capacitor not only blocks the dc voltage but also sets the low frequency cut off limit which is given by

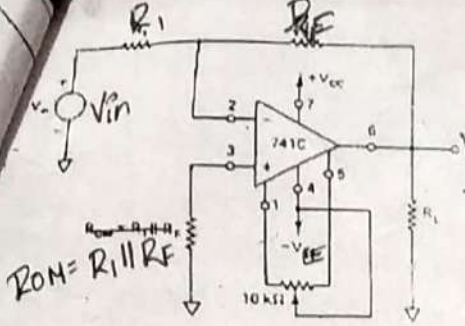
fig ③

$$f_L = \frac{1}{2\pi C_i (R_{IF} + R_O)} \rightarrow ①$$

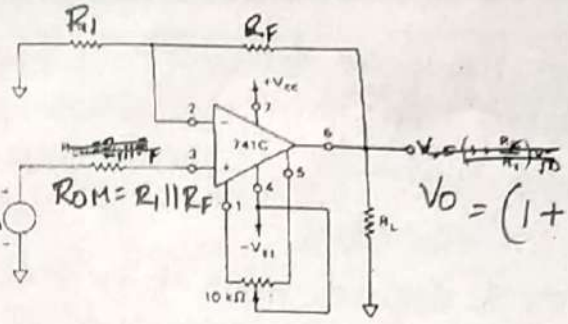
where f_L = low-frequency cutoff or low end of the bandwidth
C_i = capacitance blw two stages being coupled or dc blocking capacitor
R_{IF} = ac input resistance of the second stage
R_O = ac output resistance of first stage or the source resistance R_{in}

~~For the derivation of eqn, refer~~

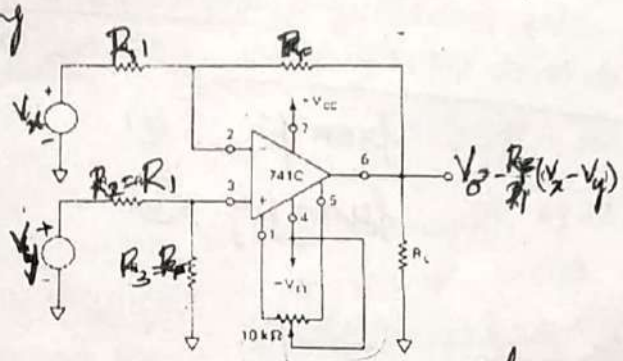
o/p offset v/g → $V_O \neq V_i$, mistake in o/p, from o/p end
I/p offset v/g → $V_O \neq V_i$, from i/p end.
I/p offset current → $I_{IOS} = I_{B_1} - I_{B_2}$
I/p bias current → $I_b = \frac{I_{B_1} + I_{B_2}}{2}$



(a) Inverting



(b) Non-inverting

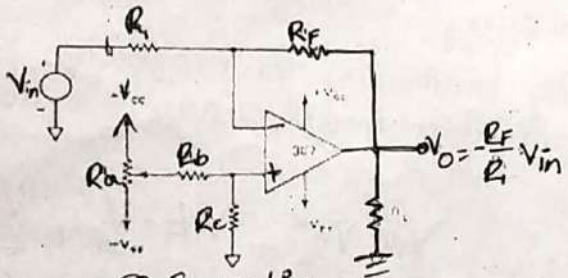


(1)

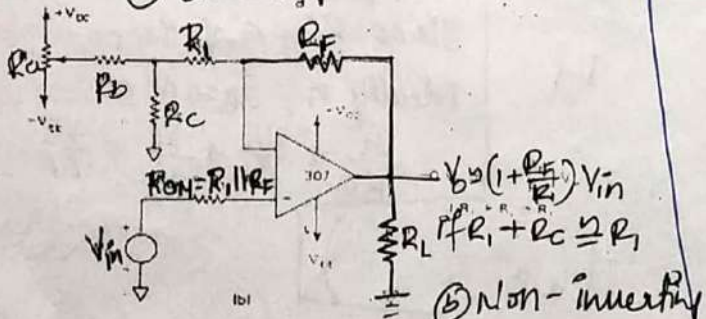
(c) Differential amp with offset null ckts

DC → only resistors

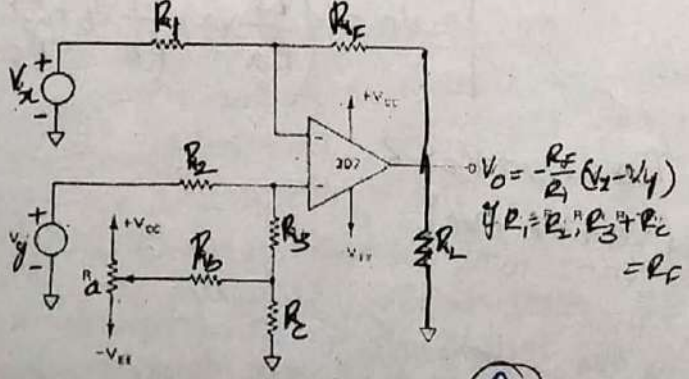
AC → capacitors, inductors



(a) Inverting

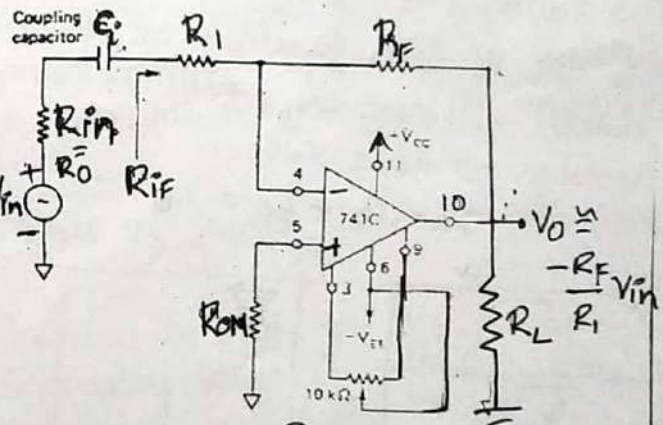


(b) Non-inverting

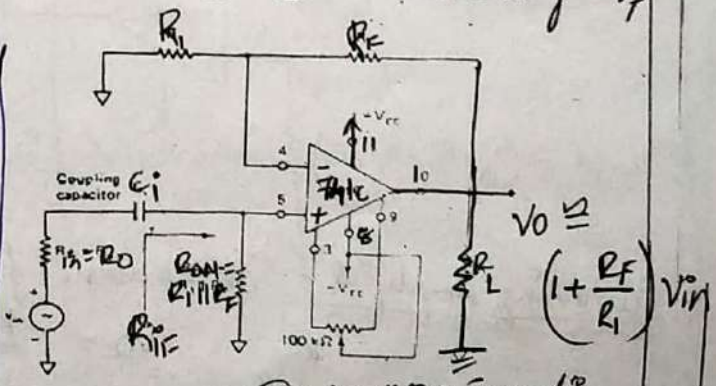


(c) Differential amp with external offset adj. ckt

(2)



(3) (a) AC inverting amp



(3) (b) AC non-inverting

(3)

C_0 → affect the BW

* The 'high-frequency cutoff f_H or high end of the bandwidth de... on the closed loop gain of the amplifier.
* Thus the bandwidth of the amplifier

$$BW = f_H - f_L$$

depends on the desired value of f_L and the closed-loop gain of the amp...
* The required value of capacitor C_i can be calculated using eq^n 1 coupling capacitor C_i, besides providing a low-frequency cutoff limit, also helps to eliminate dc d. level amplification from stage to stage.

$$A_F \cong -\frac{R_F}{R_1}$$ from fig 3 (a)

$$A_F \cong 1 + \frac{R_F}{R_1}$$ from fig 3 (b)

Summing, Scaling And Averaging Amplifiers

Inverting Configuration

* Fig shows the inverting configuration with three inputs V_a, V_b and V_c. Depending on the relationship between the feedback resistor R_F and the input resistors R_a, R_b, R_c the circuit can be used as a summing amplifier, a scaling amplifier, or an averaging amplifier.
* The circuit's function can be verified by examining the expression for the output voltage V_o which is obtained from Kirchhoff's current equation written at node V_2.

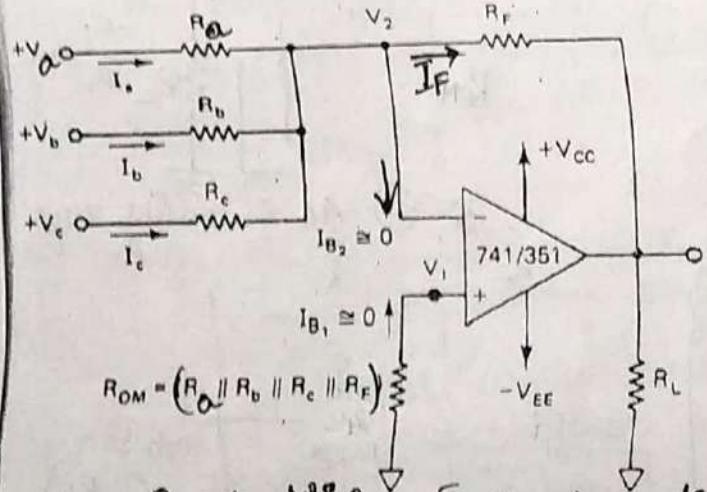
$$I_a + I_b + I_c = I_B + I_F$$

$$\frac{V_2 - V_o}{R_f} = \frac{V_a - V_2}{R_1} + \frac{V_b - V_2}{R_2} + \frac{V_c - V_3}{R_3}$$

Since $R_i \to \infty$ of the op-amp are ideally ∞, $I_B = 0$ A and $V_1 = V_2 \cong 0$ V

$V_2 = 0$

$$\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = \frac{-V_o}{R_F}$$



$$V_o = -\left(\frac{R_F}{R_a}V_a + \frac{R_F}{R_b}V_b + \frac{R_F}{R_c}V_c\right)$$

$$\therefore V_o = -\left(\frac{R_F}{R_a}V_a + \frac{R_F}{R_b}V_b + \frac{R_F}{R_c}V_c\right)$$

Summing Amplifier - In the above fig $R_a = R_b = R_c = R$

$$\therefore V_o = -\frac{R_F}{R}(V_a + V_b + V_c)$$

* This means that the output voltage is equal to the -ve sum of all the inputs times the gain of the circuit R_F/R; hence the circuit is called a summing amplifier. when the gain of the circuit is 1, that $R_a = R_b = R_c = R_F$, the output voltage is equal to the -ve sum of all input voltages

$$V_o = -(V_a + V_b + V_c)$$

Scaling or weighted amplifier

If each input voltage is amplified by a different factor, in other words weighted differently at the output. the circuit is called a scaling or weighted amplifier.

* This condition can be accomplished if R_a, R_b and R_c are different in value. Thus the output voltage of the scaling amplifier is

$$V_o = -\left(\frac{R_F}{R_a} V_a + \frac{R_F}{R_b} V_b + \frac{R_F}{R_c} V_c\right)$$

where

$$\frac{R_F}{R_a} \neq \frac{R_F}{R_b} \neq \frac{R_F}{R_c}$$

Average circuit

* The above circuit can be used as averaging circuit in which the output voltage is equal to the average of all the input voltages.

* This is accomplished by using all input resistors of equal value $R_a = R_b = R_c = R$. In addition, the gain by which each input is amplified must be equal to 1 over the number of inputs

$$\frac{R_F}{R} = \frac{1}{n}$$ where n is the number of inputs.

If 3 inputs $\frac{R_F}{R} = 1/3$

$$V_o = -\left(\frac{V_a + V_b + V_c}{3}\right)$$

* Remember that in the preceding applications the inputs V_a, V_b and V_c could be either ac or dc. These circuits are commonly used in analog computers and audio mixers in which a number of inputs is added up to produce a desired output

* In the fig Rom is used to minimize the effect of input bias currents on the output offset voltage.

* However to reduce the output offset voltage to zero, the offset voltage compensating network must be used especially when the inputs are dc voltages.

Non-inverting Configuration

If input voltages sources and resistors are connected to the non-inverting terminal. the circuit can be used either as a summing or averaging amplifier through selection of appropriate values of resistors that is R_1 and R_F.

To verify the functions of the circuit the expression for the output voltage must be obtained.

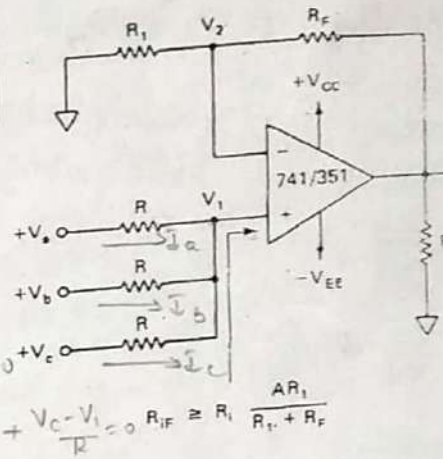
using the Superposition theorem, the voltage V_1 at the non-inverting terminal is

$$V_1 = \frac{R/2}{R+R/2} Va + \frac{R/2}{R+R/2} Vb + \frac{R/2}{R+R/2} Vc$$

$$V_1 = \frac{Va}{3} + \frac{Vb}{3} + \frac{Vc}{3} = \frac{Va+Vb+Vc}{3}$$

$$Vo = \left(1+\frac{RF}{R1}\right) V_1$$

$$Vo = \left(1+\frac{RF}{R_1}\right)\left(\frac{Va+Vb+Vc}{3}\right)$$



$$Vo = \left(1+\frac{RF}{R_1}\right) \times \left(\frac{Va+Vb+Vc}{3}\right)$$

$Ia+Ib+Ic=0$

$$\frac{Va-V_1}{R} + \frac{Vb-V_1}{R} + \frac{Vc-V_1}{R} = 0 \qquad R_{iF} \cong R_i \frac{AR_1}{R_1+R_F}$$

$$Va+Vb+Vc = 3V_1$$

Averaging Amplifier a)

The above eqn shows that the output voltage is equal to the average of all input voltages times the gain of the circuit $(1+RF/R_1)$, hence the name averaging amplifier. Depending on the application requirement the gain $(1+RF/R_1)$ can be set to a specific value. obviously, if the gain is 1, the output voltage will be equal to the average of all input voltages.

Note that there are two basic differences between this averaging amplifier and that using the inverting configuration.

1. No sign change or phase reversal occurs between the average of the inputs and output.
2. The noninverting input voltage V_1 is the average of all inputs whereas in the inverting averaging amplifier the o/p is the average of all inputs with a -ve sign.

Summing amplifier b)

★ A close examination of equation $Vo = \left(1+\frac{RF}{R_1}\right)\frac{Va+Vb+Vc}{3}$ reveals that if the gain $1+RF/R_1$ is equal to the number of inputs, the output voltage becomes equal to the sum of all input voltages. That is, if $(1+RF/R_1)=3$

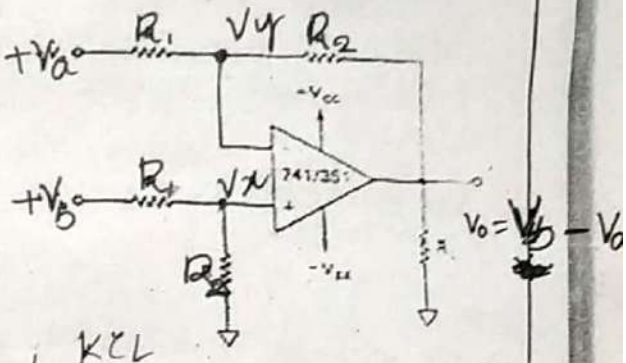
$Vo = Va+Vb+Vc$ Hence the circuit is called non-inverting summing amplifier.

★ The above fig is used as either an averaging or summing amplifier offset null circuitry or an offset null compensating network must be used to improve its accuracy.

Differential configuration

using a basic differential op-amp configuration a subtractor and a summing amplifier may be constructed

Subtractor :- a)



*A Basic differential amplifier can be used as a subtractor as shown in fig.

*Input signals can be scaled to the desired values by selecting appropriate values for the external resistors when this is done the circuit is referred to as scaling amplifier.

*However in fig all external resistors are equal in value so the gain of the amplifier is equal to 1.

$$V_o = \frac{-R}{R}(V_a - V_b)$$

$$V_o = V_b - V_a$$

*Thus o/p voltage V_o is equal to the voltage V_b applied to the non-inverting terminal minus the voltage V_a applied to the inverting terminal hence the circuit is called as subtractor.

KCL

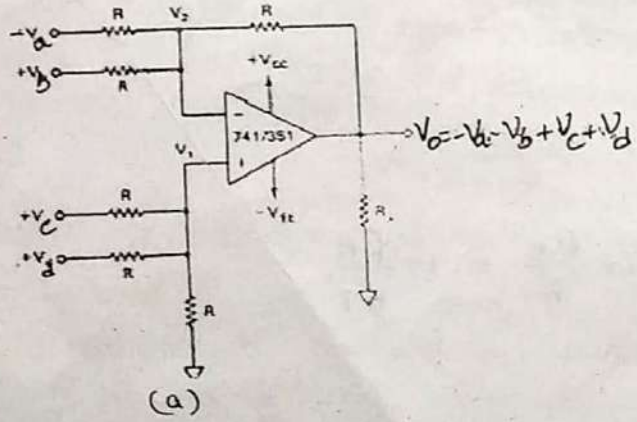
apply at node V_1, $\frac{V_2 - V_1}{R_1} = \frac{V_1 - 0}{R_2}$

$$\frac{V_2}{R_1} = \frac{V_1}{R_1} + \frac{V_1}{R_2}$$

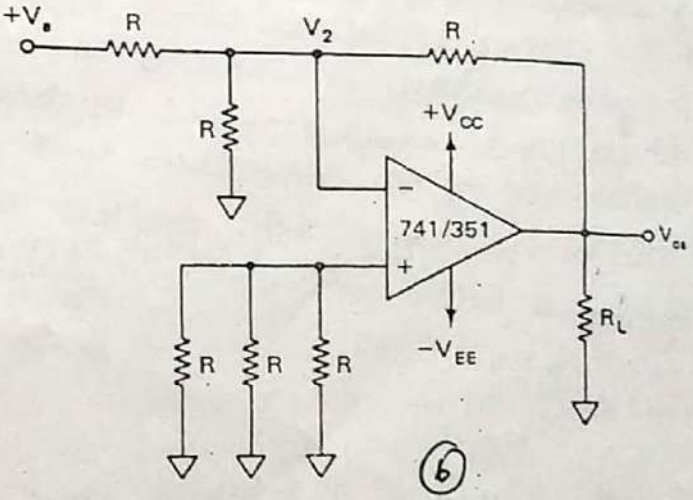
$$= V_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

$\frac{V_o}{V_{in}} = -\frac{R_f}{R_1}$

Summing amplifier :- b)



(a)



(b)

1. The four input summing amplifier may be constructed using the basic differential amplifier of fig (a) if two additional input sources are connected. one each to the inverting & non-inverting input terminals through resistor R. in fig (b)

The o/p voltage equation for this circuit can be obtained by using the superposition theorem. For instance to find the o/p voltage due to V_a alone, reduce all other input voltages V_b, V_c & V_d to zero as shown in fig (b) this circuit is inv amplifier

in which the inverting input is at virtual ground ($V_2 = 0V$)

∴ o/p voltage $V_{oa} = -\frac{R}{R} V_a = -V_a$

This result can also be obtained by Thevenizing the input circuit looking back from node V_2

$$V_{ob} = -V_b$$

I/p voltages V_a, V_b & V_d are set to zero in fig a.

$$V_1 = \frac{R/2}{R + R/2} V_c = \frac{V_c}{3}$$

o/p voltage due to V_c alone is

$$V_{oc} = \left(1 + \frac{R}{R/2}\right) V_1 = (3)\left(\frac{V_c}{3}\right) = V_c$$

o/p voltage due to input voltage V_d alone is

$$V_{od} = V_d$$

By superposition theorem

$$V_o = V_{oa} + V_{ob} + V_{oc} + V_{od}$$

$$V_o = -V_a - V_b + V_c + V_d$$

Instrumentation Amplifier using Transducer Bridge

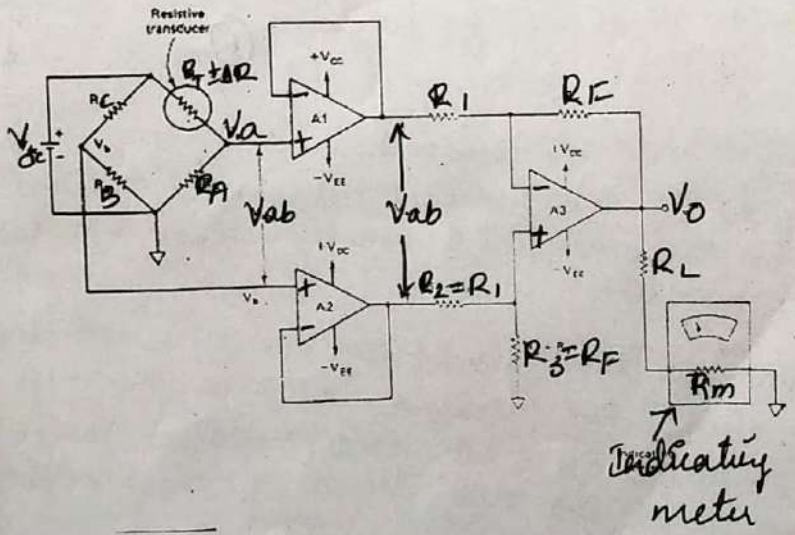
* Fig shows a simplified differential instrumentation amplifier using a transducer bridge.
* A resistive transducer whose resistance changes as a function of some physical energy is connected in one arm of the bridge with a small circle around it and is denoted by $(R_T \pm \Delta R)$ where R_T is the resistance of the transducer and ΔR the change in resistance R_T
* The bridge in fig is dc excited but could be ac excited as well

balanced bridge condition.

$$\frac{R_B (V_{dc})}{R_B + R_C} = \frac{R_A (V_{dc})}{R_A + R_T}$$

$$\Rightarrow 1 + \frac{R_B}{R_C} = 1 + \frac{R_A}{R_T}$$

$$V_b = V_a \quad (\text{or})$$



is, $\frac{R_C}{R_B} = \frac{R_T}{R_A}$

Normally, resistors R_A, R_B & R_C are selected so that they are equal in value to the transducer resistance R_T at some reference condition.

The reference condition is the specific value of the physical quantity under measurement at which the bridge is balanced.

* This value is normally established by the designer and depends on the transducer's characteristics the type of physical quantity to measured and the desired application.
* The Bridge is balanced initially at a desired reference condition.
* However, as the physical quantity to be measured changes. the resistance of the transducer also changes, which causes the bridge to unbalance ($V_a \neq V_b$)
* The o/p vtg of the bridge can be expressed as a function of the change in resistance of the transducer as described next.
* Let the change in resistance of the transducer be ΔR. Since R_B and R_C are fixed resistors, the voltage V_b is constant.
* However, voltage V_a varies as a function of the change in transducer resistance. ∴ acc to the voltage-divider rule.

$$V_a = \frac{R_A(V_{dc})}{R_A + (R_T + \Delta R)}$$

$$V_b = \frac{R_B(V_{dc})}{R_B + R_C}$$

* voltage V_{ab} across the output terminals of the bridge is

$$V_{ab} = V_a - V_b = \frac{R_A V_{dc}}{R_A + R_T + \Delta R} - \frac{R_B V_{dc}}{R_B + R_C}$$

* however, if $R_A = R_B = R_C = R_T = R$ then

$$V_{ab} = -\frac{\Delta R\,(V_{dc})}{2(2R + \Delta R)} = \frac{\Delta R\,(V_{dc})}{2(2R + \Delta R)}$$

* -ve sign indicates that $V_a < V_b$ because of the increase in the value of ΔR
* The output voltage V_{ab} of the bridge is then applied to the differential Instrumentation amplifier composed of 3 op-amps.
* The voltage follower preceeding the basic differential amplifier help to eliminate loading of the bridge circuit.
* The gain of the basic differential amplifier is $(-R_F/R_1)$;

$$V_o = V_{ab}\left(-\frac{R_F}{R_1}\right) = \frac{(\Delta R)V_{dc}}{2(2R + \Delta R)} \quad \frac{R_F}{R_1}$$

* The change in resistance of the transducer ΔR is very small. ∴ we can approximate $(2R + \Delta R) \cong 2R$

$$V_o = \frac{R_F}{R_1}\frac{\Delta R}{4R} V_{dc}$$

* The eqn indicates that v_o is directly proportional to the change in ΔR of the transducer.
* Since the change in resistance is caused by a change in physical energy a meter connected at the output can be calibrated in terms of the unit of that physical energy.
* Before proceeding with specific bridge applications, let us briefly consider the important characteristics of some resistive types of transducers. In these resistive types of transducers the resistance of the transducer changes as a function of some physical quantity.
* Thermistors, photoconductive cells and strain gages are some of the most commonly used resistive transducers; hence they will be futher discussed here.
* Thermistors are essentially semiconductors that behave as resistors usually with a negative temperature co-efficient of resistance. i.e, as the temperature of a thermistor increases, its resistance decreases.
* The temperature co-efficient of resistance is expressed in ohms per unit change in degrees Celsius.
* Thermistor with high temperature co-efficient of resistance are more sensitive to temp change and ∴ well suited to temp measurement and control.
* Thermistors are available in a wide variety of shapes and sizes However the thermistor beads sealed in the tips of glass rods are most commonly used because they are relatively easy to mount.
* The photoconductive cell belongs to the family of photodetectors whose resistance varies with an incident radiant energy or with light.
* As the intensity of incident light increases the resistance of the cell decreases.
* The resistance of the photoconductive cell in darkness is typically on the order of 100KΩ.
* Generally, the resistance of the cell in darkness and at particular light intensities is listed on the data sheet. The intensity of light is expressed in meter candles (lux).
* Materials such as cadmium sulfide and silicon, whose conductivity is a function of incident radiant energy are used for photoconductive cells.
* Some cells are extremely sensitive to light and hence can be used into the ultraviolet & infrared regions.
* The photoconductive cell is typically composed of a ceramic base a layer of photoconductive material, a moisture-proof enclosure and metallic leads. Photoconductive cells are also known as photocells or light dependent resistors.

Another important resistive transducer is the strain gage. whose resistance changes due to elongation or compression when an external stress is applied.
The stress is defined as force per unit area (newtons/(meter)^2) and can be related to pressure, torque and displacement.
* ∴, a strain gage may be used to monitor change in applied pressure, torque and displacement by measuring the corresponding change in the gage's resistance.
* Two basic types of strain gage's are wire and semiconductor. Semiconductor strain Gages are much more sensitive than the wire type and ∴ provide better accuracy and resolution.
* The sensitivity of a strain gage is defined as unit change in resistance per unit change in length and is a dimensionless quantity.
* The thermistor, photocell, and strain gage are all passive transducers, meaning that they require external voltage for their operation.

Applications of Instrumentation amplifier –

Temperature indicator a)

* The above circuit can be used as a temp indicator if the transducer in the bridge circuit is a thermistor and the o/p meter is calibrated in degrees celsius or Fahrenheit.
* The bridge can be balanced at a desired reference condition for instance 25°C. As the temperature varies from its reference value, the resistance of the thermistor changes and the bridge becomes unbalanced.
* This unbalanced bridge in turn produces the meter movement.
* The meter can be calibrated to read a desired temp range by selecting an appropriate gain for the differential instrumentation amplifier.
* In the above fig meter movement is dependent on the amount of imbalance in the bridge that is the change ΔR in the value of the thermistor resistance.
* The ΔR for the thermistor. however can be determined as follows

ΔR = (temp co-efficient of resistance) (final temp – reference temp)

Temperature controller b)

* A simple and inexpensive temp control circuit may be constructed by using a thermistor in the bridge circuit and by replacing a meter with a relay in the circuit. of ↑ above fig.
* The o/p of the differential instrumentation amplifier drives a relay that controls the current in the heat-generating circuit. A properly designed circuit should energize a relay when the temp of the thermistor drops below a desired value. causing the heat unit to turn on.

Light Intensity meter: c)

* The circuit in the above fig can be used as a light intensity meter if a transducer is a photocell.
* The bridge can be balanced for darkness conditions. ∴ when exposed to light the bridge will be unbalanced and cause the meter to deflect in proportion to the change in light intensity.
* The meter can be calibrated interms of lux to measure the change in light intensity.
* The light-intensity meter using an instrumentation bridge amplifier is more accurate and stable than single-input inverting / non inverting configurations because the common-mode (noise) voltages are effectively rejected by differential configuration.

Measurement of flow and thermal conductivity d)

* A flow meter or a thermal conductivity meter may be constructed using the circuit of the above fig. provided that two thermistors are used adjacent to each other in the bridge.
* For instance, assume that R_C and R_T represent two identical thermistors
* For the flow measurement, one thermistor is sealed in a small cavity copper cylinder and the other installed in a small copper pipe.
* when no air flows through the pipe, the bridge can be balanced so that the output voltage is zero when air flows over the thermistor its ~~thermal~~ temp decreases and in turn the resistance increases causing the bridge to be unbalanced
* This unbalanced voltage is then amplified by the differential instrumentation amplifier and applied to the meter.
* Thus the amount of meter deflection is proportional to the flow rate of the air in the pipe
* The meter can be calibrated in (meter)^3/second to accommodate a desired flow, rate range.
* For the thermal conductivity measurement, two thermistors are mounted in seperate small copper cylinders. with air in both cylinders the bridge can be balanced and hence the output will be zero.
* when air in one cylinder is replaced by a medium being tested which has a different thermal conductivity than air, thermistor changes thus changing its resistance.
* Suppose that the medium being tested is CO_2. Because of its lower thermal conductivity CO_2 will increase the temperature of the thermistor which will cause a decrease in the thermistor's resistance. This results in unbalancing the bridge which in turn produces a meter deflection.

Analog weight Scale c)

By connecting a strain gage in the bridge. the circuit in above fig can be converted into a simple and inexpensive analog weight scale.

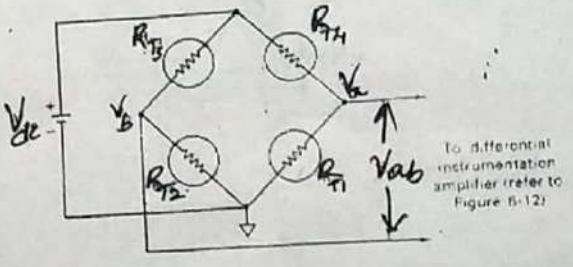
* In the analog weight scale, strain gage elements are connected in all four arms of the bridge.
* The elements are mounted on the base of the weight platform so that when an external force or weight is applied to the platform, one pair of elements in the opposite arms elongates, whereas the other pair of elements in the opposite arms compresses.
* In other words, when the weight is placed on the platform R_{T1} and R_{T3} both decrease in resistance and R_{T2} and R_{T4} both increase in resistance, or vice versa.
* when no weight is placed on the platform, the bridge is balanced $R_{T1} = R_{T2} = R_{T3} = R_{T4} = R$ and the o/p voltage of the weight scale can be zero.
* when a weight is placed on the scale platform the bridge becomes unbalanced
* Assuming that R_{T1} and R_{T3} decrease in resistance and R_{T2} and R_{T4} increase in resistance by the same number of ohms ΔR, the unbalanced voltage V_{ab} is given by $V_{ab} = -V_{dc}\left(\frac{\Delta R}{R}\right)$
* where V_{dc} = dc excitation voltage of the bridge

$R = R_{T1} = R_{T2} = R_{T3} = R_{T4}$ = unstrained gage resistance

ΔR = change in gage resistance.

* Remember that, if the decrease in gage resistance R_{T1} & R_{T3} is ΔR, the increase in resistance of R_{T2} and R_{T4} is also ΔR. ∴ with this assumption the voltage $V_a < V_b$ and the output voltage V_{ab} is negative as indicated by eqn $V_{ab} = -V_{dc}\left(\frac{\Delta R}{R}\right)$
* The voltage V_{ab} is then amplified by differential instrumentation amplifier which drives the meter, since the gain of the amplifier is $(-R_F/R_1)$, the output voltage V_o is

$$V_o = V_{dc}\left(\frac{\Delta R}{R}\right)\frac{R_F}{R_1}$$



* For better accuracy and resolution, a microprocessor-based digital weight scale may be constructed However such a scale is much more complex and expensive than the analog scale.
* The gain of the amplifier can be selected acc to the sensitivity of the strain gage and the full-scale deflection requirements of the meter. The meter can be calibrated in terms of kilograms.

Basic Comparator

fig ① & ②

★ Figure ① shows an op-amp used as a comparator. A fixed reference voltage V_{ref} of 1V is applied to the (−) input and the other time-varying signal voltage V_{in} is applied to the (+) input.

★ Because of this arrangement the circuit is called non-inverting comparator.

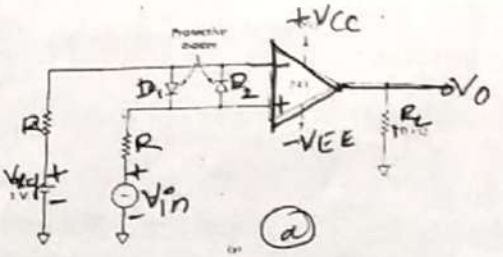
★ When V_{in} is less than V_{ref}, the output voltage V_o is at $-V_{sat}$ ($\cong -V_{EE}$) because the voltage at the (−) input is higher than that at the (+) input.

★ On the other hand, when V_{in} is greater than V_{ref} the (+) input becomes positive wrt (−) input, the V_o goes to $+V_{sat}$ ($\cong +V_{cc}$). Thus V_o changes from one saturation level to another whenever $V_{in} \cong V_{ref}$ as shown in fig b.

In short, the comparator is a type of analog-to-digital converter.

At any given time the V_o waveform shows whether V_{in} is greater or less than V_{ref}.

The comparator is sometimes also called a voltage-level detector because for a desired value of V_{ref} the voltage level of the input V_{in} can be detected.



(a)

(a) Non-inverting comparator

(b) $V_{ref} \rightarrow +Ve$

(c) $V_{ref} \rightarrow -Ve$

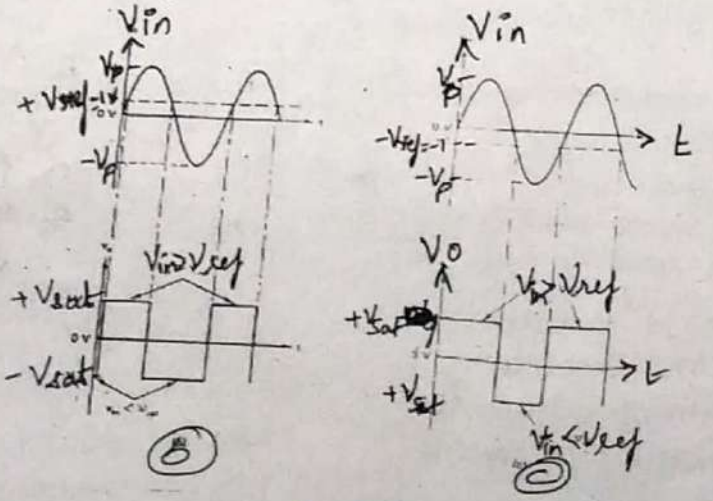


fig ①

fig a the diodes d_1 & d_2 protect the op-amp from damage due to excessive voltage vin. Because of these diodes, the difference input voltage vid the op-amp is clamped to either 0.7V or -0.7V; hence the diodes are called clamp diodes.

* There are some op-amps with built-in input protection; in such op-amps the input diodes d_1 & d_2 are unnecessary.
* The resistance R is in series with Vin is used to limit the current through D_1 & D_2.
* To reduce offset problems, a resistance $R_{om} \cong R$ is connected blw the (-) input and Vref.
* If the reference voltage Vref is negative with respect to ground. with a sinusoidal signal applied to the (+) input, the output waveform will be as shown in fig c.
* when $V_{in} > V_{ref}$ V_o is at $+V_{sat}$ on the other hand when $V_{in} < V_{ref}$ V_o is at $-V_{sat}$. obviously the amplitude of Vin must be large enough to pass through Vref if the switching action is to take place.
* Fig (2) in next diagram shows an inverting comparator in which the reference voltage Vref is applied to the (+) input and Vin is applied to the (-) input
* In this circuit Vref is obtained by using a 10KΩ potentiometer that forms a voltage divider with dc supply voltages $+V_{cc}$ & $-V_{EE}$, Vref becomes more negative. while if it is moved toward $+V_{cc}$, Vref becomes more +ve
* Thus a Vref of a desired amplitude and polarity can be obtained by simply adjusting the 10KΩ potentiometer.
* with the sinusoidal input waveform the output V_o has the waveform shown in fig b or c in next diagram depending on whether Vref is +ve or -ve respectively.

Zero-crossing Detector

* An immediate application of comparator is the zero crossing detector or sine wave to square wave converter.
* The basic comparator of fig a in the above diagram & the next diagram can be used as the zero crossing detector provided that Vref is set to zero.
* Fig a in (3) diagram shows the inverting comparator used as a zero crossing detector.
* The output voltage V_o waveform in fig b of 3rd diagram shows when and in what direction an input signal Vin crosses zero volts
* That is, o/p V_o is driven into -ve saturation when the input signal Vin passes through zero in +ve direction. conversly when Vin passes through zero in the -ve direction, the o/p V_o switches & saturates +ve.

* In some applications, the i/p vin may be a slowly changing waveform that a low frequency signal, the input vin may be a ~~slowly~~ changing mo
* ∴ it will take vin more time to cross 0v. therefore V_o may not swi quickly from one saturation voltage to the other.
* on the other hand, because of noise at the op-amp's input terminals the output V_o may fluctuate b/w 2 saturation voltages $+V_{sat}$ & $-V_{sat}$ at detecting zero reference crossings for noise voltages as well as Vin.
* Both of these problems can be cured with the use of regenerative or +ve feedback that causes the o/p V_o to change faster and eliminate any false o/p transitions due to noise signals at the input.

Schmit Trigger

* Fig 4a shows an inverting comparator with +ve feedback.
* This circuit converts an irregular-shaped waveform to a square wave or pulse.
* The circuit is known as the Schmitt trigger or squaring circuit.
* The input voltage Vin triggers the o/p V_o every time it exceeds certain voltage levels called upper threshold voltage V_{ut} and lower threshold voltage V_{lt}.

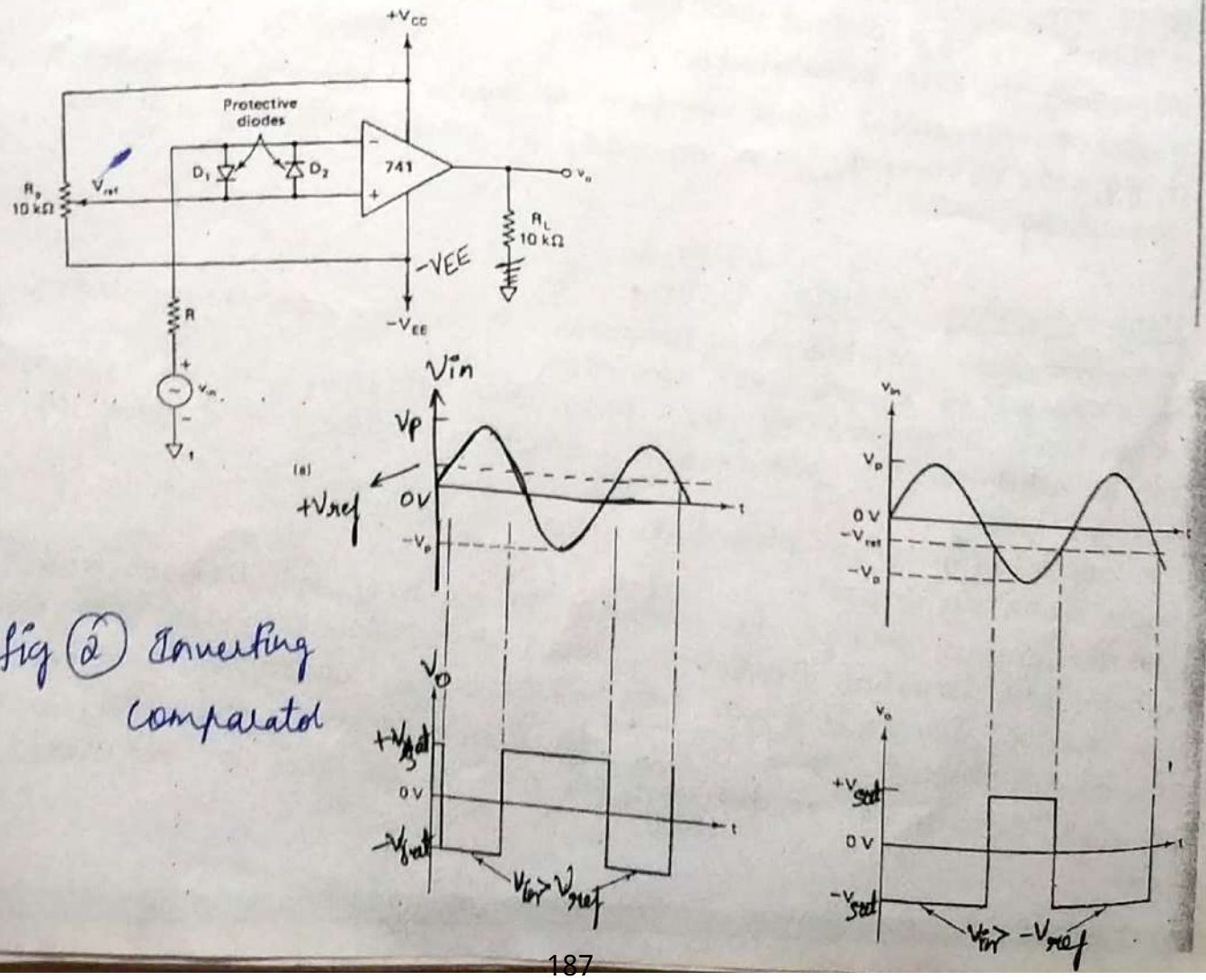
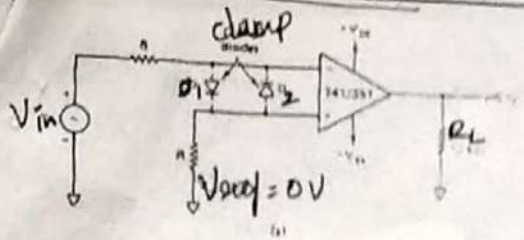
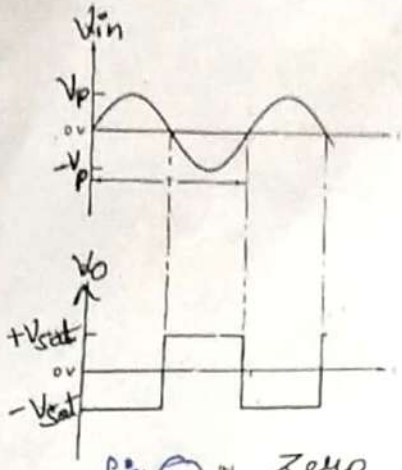


fig (2) Inverting comparator

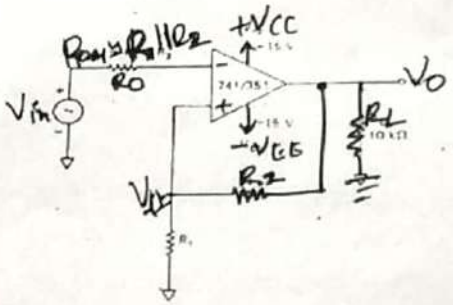


(a)

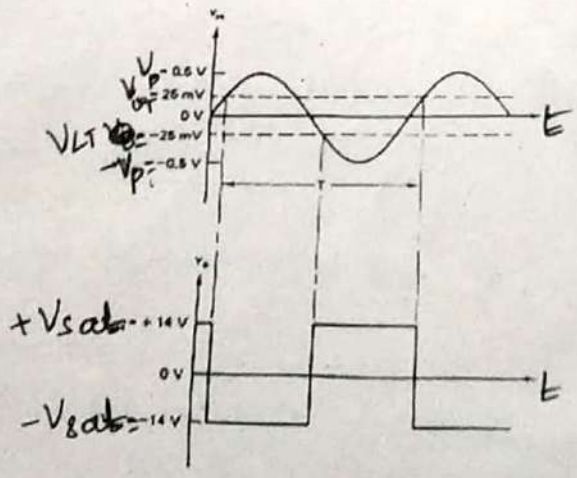


(b)

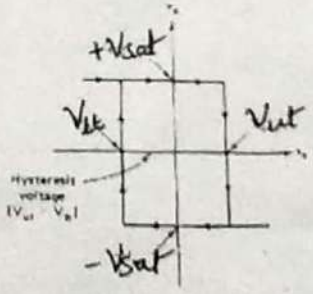
fig (3) zero crossing detector



(a)



(b)



(c)

Inverting comparator as Schmitt Trigger

* In fig 4a threshold voltages are obtained by using the voltage divider R_1, R_2 where the voltage across R_1 is fed back to the (+) input. The voltage across R_1 is a variable reference threshold voltage that depends on the value and polarity of the output voltage v_o

* when $v_o = +V_{sat}$ the voltage across R_1 is called the upper threshold voltage V_{ut}. The input voltage v_{in} must be slightly more +ve than V_{ut} in order to cause the o/p v_o to switch from $+V_{sat}$ to $-V_{sat}$

using the voltage-divider rule.

$$V_{ut} = \frac{R_1}{R_1+R_2}(+V_{sat})$$

* on the other hand, when $v_o = -V_{sat}$, the voltage across R_1 is referred to as lower threshold voltage, V_{lt}. v_{in} must be slightly more negative than V_{lt} in order to cause v_o to switch from $-V_{sat}$ to $+V_{sat}$ In other words, for v_{in} values greater than V_{lt}, v_o is at $-V_{sat}$. V_{lt} is given by the following equation:

$$V_{lt} = \frac{R_1}{R_1+R_2}(-V_{sat})$$

* Thus, if the threshold voltages V_{ut} and V_{lt} are made larger than the input noise voltages, the positive feedback will eliminate the false output transitions. Also the +ve feedback, because of its regenerative action will make v_o switch faster b/w $+V_{sat}$ & $-V_{sat}$ fig 4a resistance $R_{om} \cong R_1 \| R_2$ is used to minimize the offset problems.

* Fig 4b shows that the o/p of the Schmitt trigger is a square wave when the input is a sine wave. Recall that a slightly different version of the schmitt trigger is used in the triangular wave & sawtooth wave generators

In ~~the~~ ge

** Generators a noninverting comparator is used as schmitt trigger is a

* when the i/p is a triangular wave the output of the schmitt trigger is a square wave. whereas if the input is a sawtooth wave the o/p is a pulse waveform.

* The comparator with +ve feedback is said to exhibit hysteresis, a deadband condition.

* That is, when the i/p of the comparator exceeds V_{ut}, its output switches from $+V_{sat}$ to $-V_{sat}$ and reverts back to its original state. $+V_{sat}$. when the input goes below V_{lt}: The hysteresis voltage is of course equal to the difference between V_{ut} & V_{lt}:

$$V_{hy} = V_{ut} - V_{lt}$$

$$V_{hy} = \frac{R_1}{R_1+R_2}[+V_{sat} - (-V_{sat})]$$

MODULE #5

Two chapters of module 5 are as follows:

1. Op-amp circuits ✓
2. 555 Timer and its Applications

8.11 Analog to Digital and Digital to Analog converters

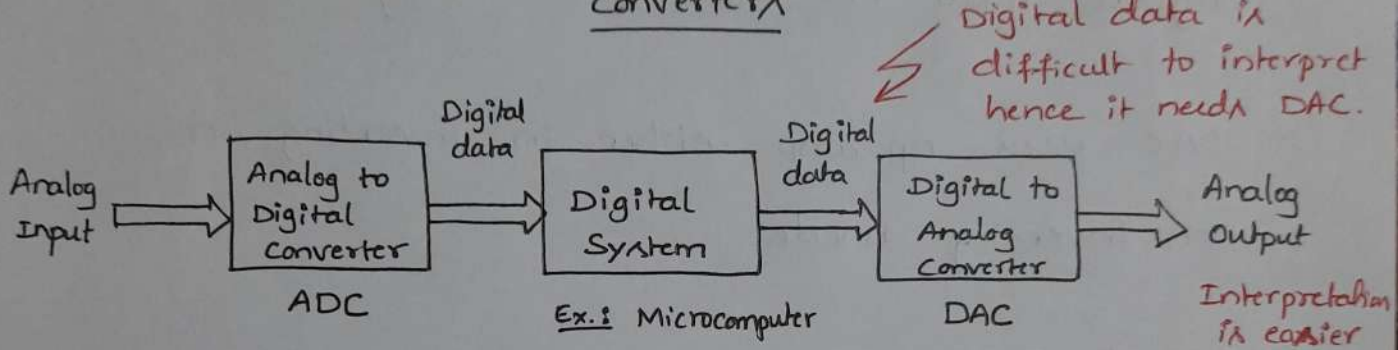


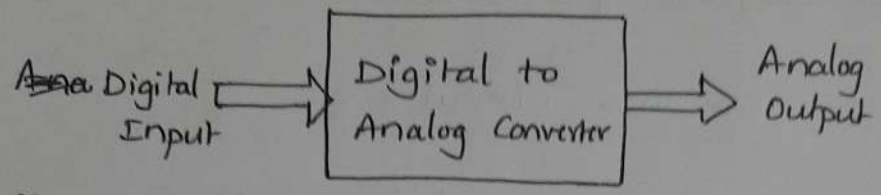
Fig. 1. Block Diagram of ADC and DAC

→ Fig. 1. shows the block diagram of analog to digital and digital to analog conversion.

→ The digital system employed between ADC and DAC may be a microcomputer which processes digital data.

→ The digital data processing have the following advantages: (i) Efficient
(ii) Reliable, and
(iii) Economic

8.11.1. Digital to Analog Converters



Definition:

A digital to analog converter (DAC) converts digital input (0s and 1s) to analog output.

→ DAC uses op-amp either in inverting or non-inverting mode.

Types of DAC: Two types of DACs are as follows:

1. Binary weighted Resistors
2. R-2R Resistors

8.11.1(a): D/A Converter with Binary Weighted Resistors

→ Fig. 2. shows D/A converter using an op-amp and binary weighted resistors.

→ Op-amp connected in: Inverting mode

However, op-amp can also be connected in Non-inverting mode.

→ No. of Binary inputs considered : 04

Therefore, the D/A converter is 4-bit

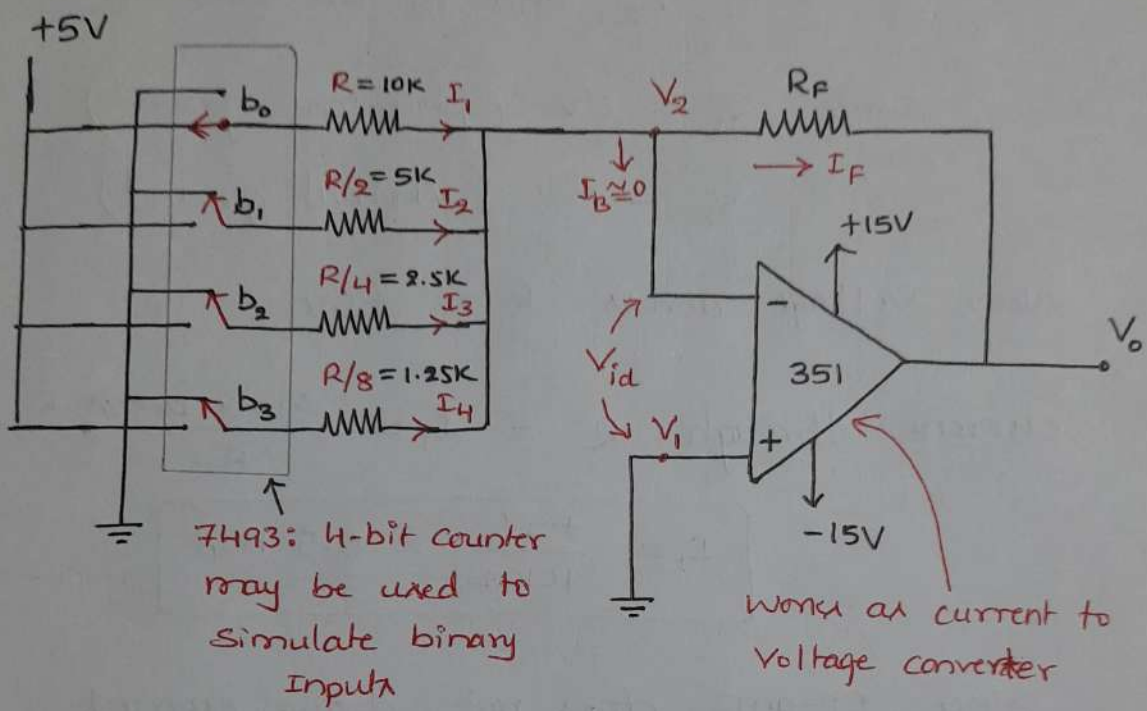


Fig. 2. D/A Converter with Binary Weighted Resistors

→ Since No. of inputs = 04

possible combination : $2^4 = 16$

b_3	b_2	b_1	b_0	
0	0	0	0	16 combinations
0	0	0	1	
0	0	1	0	
⋮				
1	1	1	1	

D/A Conversion Example

(i) $b_3\ b_2\ b_1\ b_0 \equiv 0001$

i.e b_0 is connected to +5V

b_1, b_2, and b_3 are connected to 0V

Since $V_1 = 0V$ (physical ground)

$V_2 = 0V$ (virtual ground)

Now Voltage across $R = +5V$

current through $R = I_1 = \dfrac{\text{Voltage across } R}{R}$

$$I_1 = \frac{+5V}{10K\Omega} = 0.5\ mA$$

Since Op-amp does not draw current

i.e $I_B \cong 0$

$\Rightarrow$ I_F = current through Feedback resistor

$I_F = I_1$ Since $I_B \cong 0$

$$I_F = 0.5\ mA$$

Output Voltage = $V_o = V_2 - \text{Drop across } R_F$

$V_2 = 0V$ (Virtual ground)

$V_o = 0 - I_F \times R_F = -0.5\ mA \times 1K\Omega$

$$V_o = -0.5V$$

(ii) $b_3 b_2 b_1 b_0 = 0010$

i.e b_1 is connected to +5V

b_3, b_2, and b_0 are connected to ground (=0V)

$I_1 = I_3 = I_4 = 0$

current through $R/2 = I_2 = \dfrac{\text{Voltage across } R/2}{R/2}$

Therefore, $\boxed{I_2 = \dfrac{+5V}{10K/2} = 1\ mA}$

Since $I_F = I_2 = 2I_1$

$V_0 = 0 - I_F \times R_F = -1\ mA \times 1K\Omega = -1V$

$\boxed{V_0 = -1V}$

(iii) $b_3 b_2 b_1 b_0 = 0011$

$I_1 = 0.5\ mA$

$I_2 = 1\ mA$

$I_F = I_1 + I_2 = 0.5 + 1 = 1.5\ mA$

$V_0 = -I_F \times R_F = -1.5 \times 1K\Omega = -1.5V$

$\boxed{V_0 = -1.5V}$

→ Depending on b_0, b_1, b_2, and b_3 switches open or close binary weighted currents are set-up in the input resistors.

→ Sum of these binary weighted currents are equal to the current flowing through R_F

→ The proportional output voltage is calculated based on these binary weighted currents.

→ When all the switches are closed, output will be maximum. The V_o equation is given by

$$V_o = -R_F \left(\frac{b_0}{R} + \frac{b_1}{R/2} + \frac{b_2}{R/4} + \frac{b_3}{R/8} \right)$$

where b_0, b_1, b_2 and b_3 are 0V or +5V

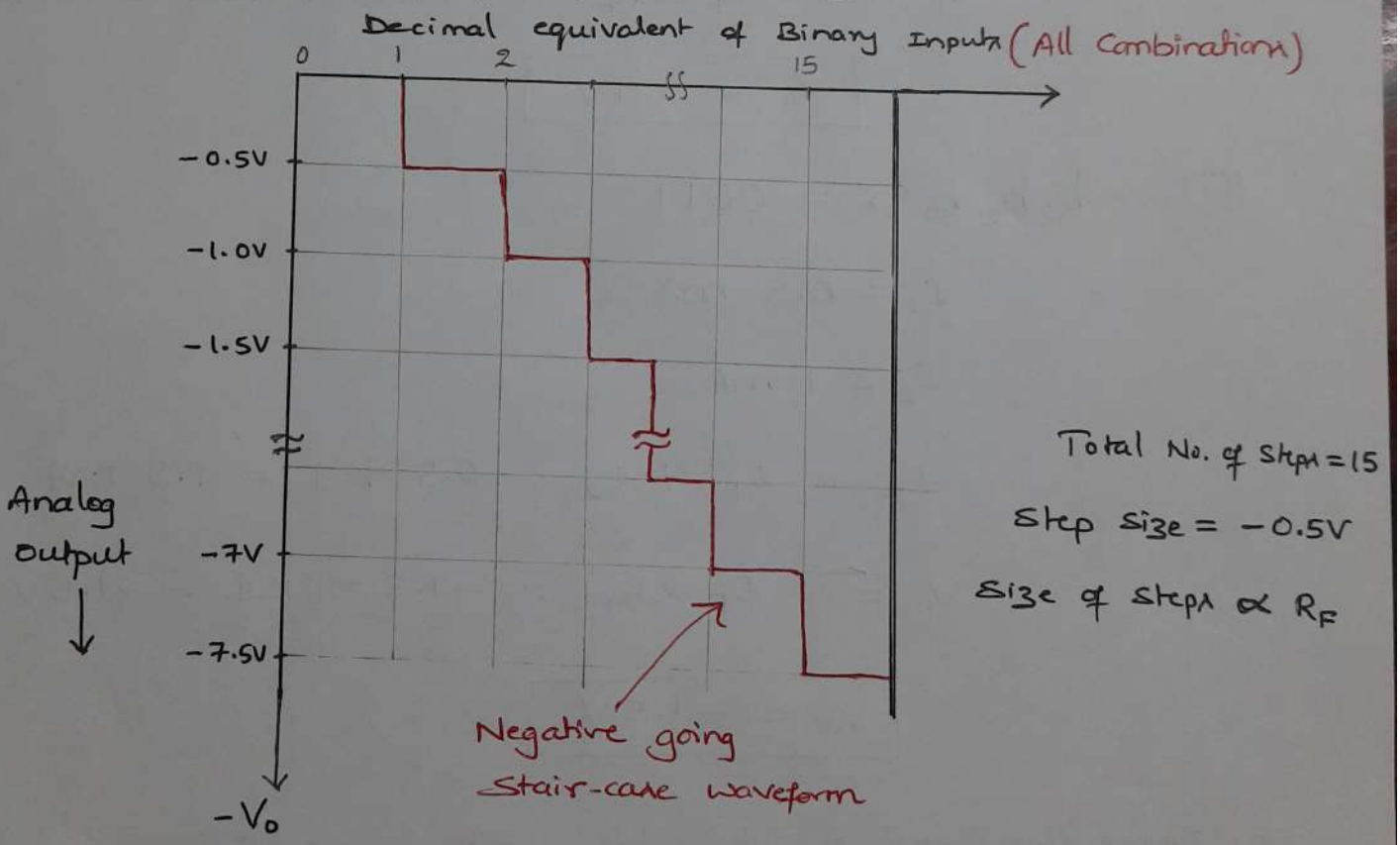


Fig. 3. Graph of Digital Input Versus Analog Output

Note: max. output voltage of an op-amp = $\pm V_{sat}$

Disadvantage

→ Requires Binary weighted Resistors

i.e for more no. of inputs (i.e Digital inputs > 4)

more resistor combinations are required

⇒ practically not feasible

Solution: Use R-2R D/A Converter

8.11.1 (b) D/A Converter with R and 2R Resistors

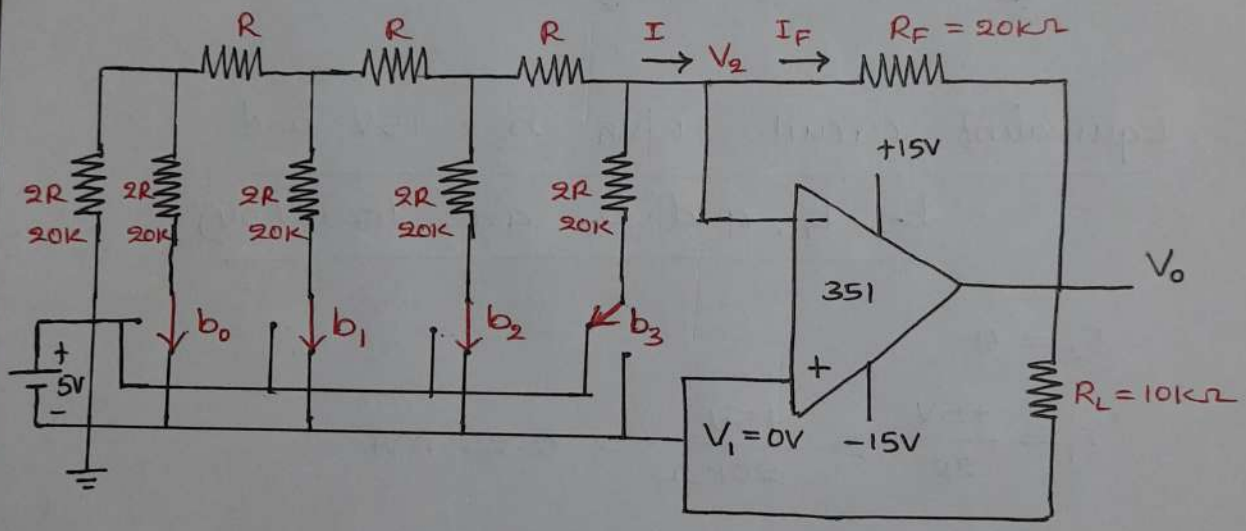


Fig. 4. D/A Converter with R and 2R Resistors

→ Fig. 4 shows the circuit diagram of D/A converter with R and 2R resistors.

→ $b_3\ b_2\ b_1\ b_0$: Binary inputs, simulated through switches

→ $V_o \propto$ Binary Inputs and $b_3 b_2 b_1 b_0$ can be 0V or +5V

Example: (i) Assume $b_3 b_2 b_1 b_0 = 1000$

i.e b_3 : connected to +5V

b_2, b_1, and b_0 : connected to 0V

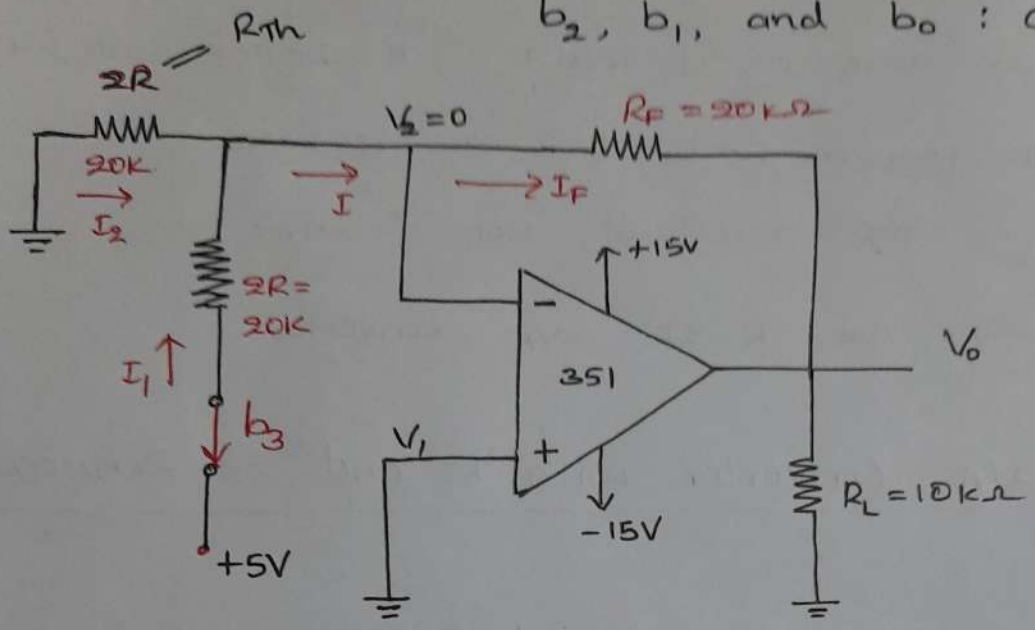


Fig. 5 Equivalent circuit when b_3 = +5V and b_2, b_1, and b_0 are low (0V)

$$I_2 = 0$$

$$I_1 = \frac{+5V}{2R} = \frac{+5V}{20K\Omega} = 0.25\ mA$$

$$R_{Th} = \left[\left\{\left[(2R \| 2R + R) \| 2R\right] + R\right\} \| 2R\right] + R = 2R = 20K\Omega$$

$V_2 = 0V$ (Virtual ground)

$I_2 = 0\ mA$, $I_1 = 0.25\ mA = I_F = I$

$V_0 = -I_F \times R_F = -0.25mA \times 20K\Omega$

$$\boxed{V_0 = -5V}$$

III^{r} procedure can be used to calculate output voltage for all possible input combinations.

(ii) For $b_3 b_2 b_1 b_0 = 1111$

The output for this combination is called max. or Full-scale output

The Full-scale output can be calculated using the following equation:

$$V_0 = -R_F \left(\frac{b_3}{2R} + \frac{b_2}{4R} + \frac{b_1}{8R} + \frac{b_0}{16R} \right)$$

where b_3, b_2, b_1 and b_0 can be 0V or +5V

For $b_3 b_2 b_1 b_0 = 1111$, the above equation becomes

$$V_0 = -20K \left(\frac{5V}{20K} + \frac{5V}{40K} + \frac{5V}{80K} + \frac{5V}{160K} \right)$$

$$= -20K \left(\frac{5\times8 + 5\times4 + 5\times2 + 5\times1}{160K} \right)$$

$$= -20K \left(\frac{40 + 20 + 10 + 5}{160K} \right)$$

$$= -\frac{75}{8} = -9.375$$

$$V_0 = -9.375$$

Decimal equivalent of Binary Inputs	Input (V) b_3	b_2	b_1	b_0	output Voltage (V)
0	0	0	0	0	0
1	0	0	0	5	−0.625
2	0	0	5	0	−1.25
3	0	0	5	5	−1.875
4	0	5	0	0	−2.50
5	0	5	0	5	−3.125
6	0	5	5	0	−3.750
7	0	5	5	5	−4.375
8	5	0	0	0	−5V
9	5	0	0	5	−5.625
10	5	0	5	0	−6.25
11	5	0	5	5	−6.875
12	5	5	0	0	−7.50
13	5	5	0	5	−8.125
14	5	5	5	0	−8.875
15	5	5	5	5	−9.375

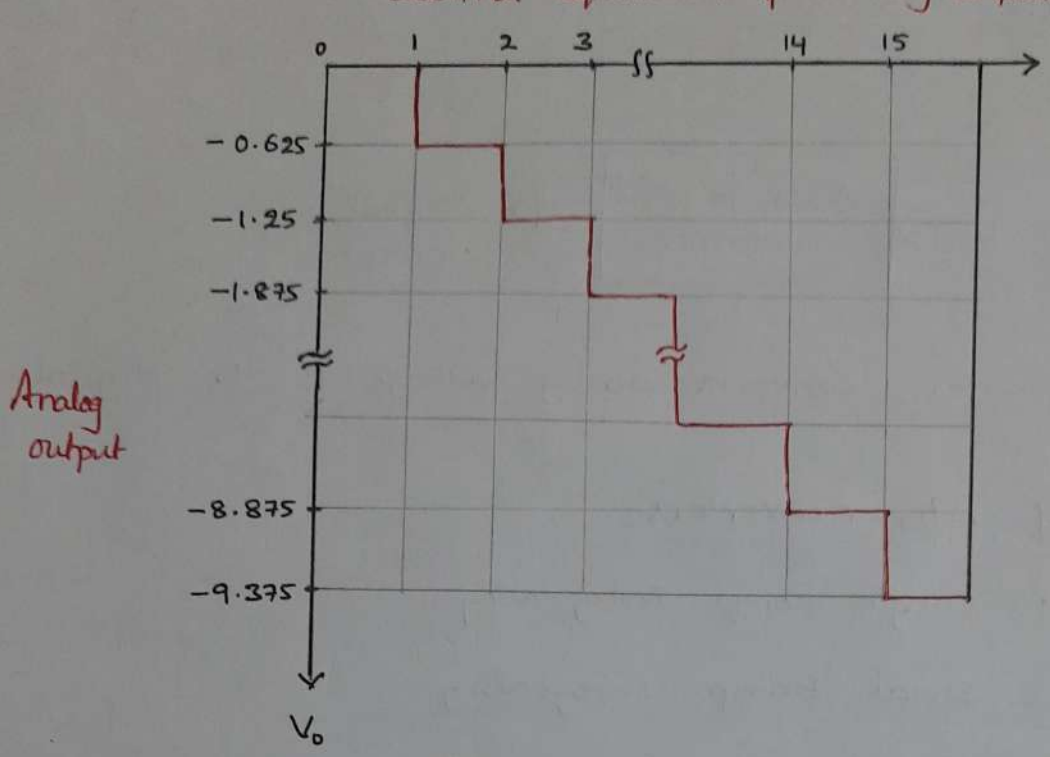


Fig. 5. Output Versus Input

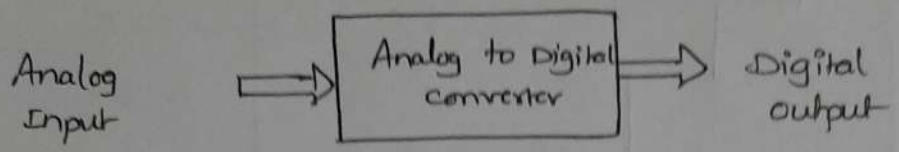
Advantages:

Requires two set of precision resistances

Disadvantages

1. More resistances, more difficult to analyze, then binary weighted resistor type.
2. For more than four digital inputs
   - Both circuit becomes complex
   - Accuracy decreases.

8.11.2 A/D Converters



A/D converter converts analog voltage to the digital output

Types of A/D Converters:

1. Single Ramp Integrating
2. Dual Ramp Integrating
3. Single Counter
4. Tracking
5. Successive Approximation type A/D converter

8.11.2 (a) Successive Approximation Type A/D Converter

→ Fig. 6. shows the successive approximation type A/D Converter.

→ Heart of the circuit : 8-bit successive approx. Register (SAR)

→ Output of SAR = 8-bit DAC

→ Output of DAC is compared with analog input, V_{in}

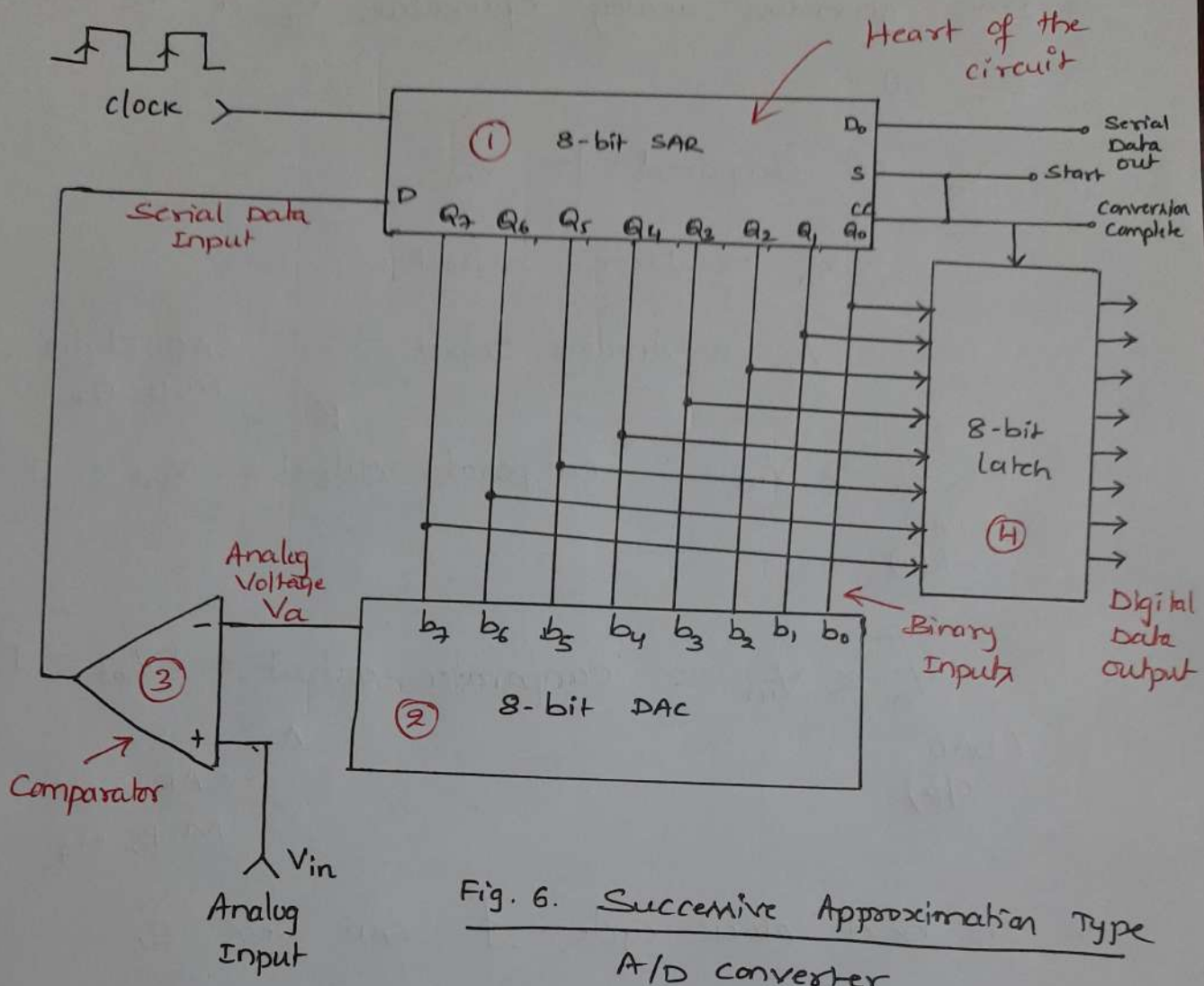


Fig. 6. Successive Approximation Type A/D converter

→ 8-bit latch holds 8-bit digital data output at the end of conversion.

Working:

→ Apply Start of conversion signal, S as high

⟹ SAR is reset

→ For first clock cycle (⎍), Q_7 of SAR is set to '1'

→ DAC generates analog equivalent V_a to the Q_7 bit

→ V_a is compared to V_{in}

V_a = DAC output

V_{in} = Analog Input

SAR clears MSB, Q_7

$V_a > V_{in}$: comparator output = $-V_{sat}$ = '0'

(DAC o/p)

$V_a < V_{in}$: comparator output = $+V_{sat}$ = '1'

(DAC o/p)

SAR sets MSB, Q_7

→ In next clock cycle, ↑ SAR sets Q_6

Now, depending on output of comparator, SAR either keep or reset bit Q_6

→ This process is continued until SAR tries all bits.

→ As soon as LSB, Q_0 is tried

SAR forces conversion complete cc to high

→ The cc signal enables latch and digital data appears at the output of latch.

→ Digital data is available serially as SAR determines each bit.

→ cc connected to start of conversion converts continuously analog to digital

→ 8-bit successive approximation type A/D converter requires 8-bit clock cycles.

8.12.2 SMALL-SIGNAL HALF-WAVE RECTIFIERS

(Also called as Precision Rectifiers)

→ Rectifier circuits, namely half-wave, full-wave, and bridge can be constructed using normal diodes.

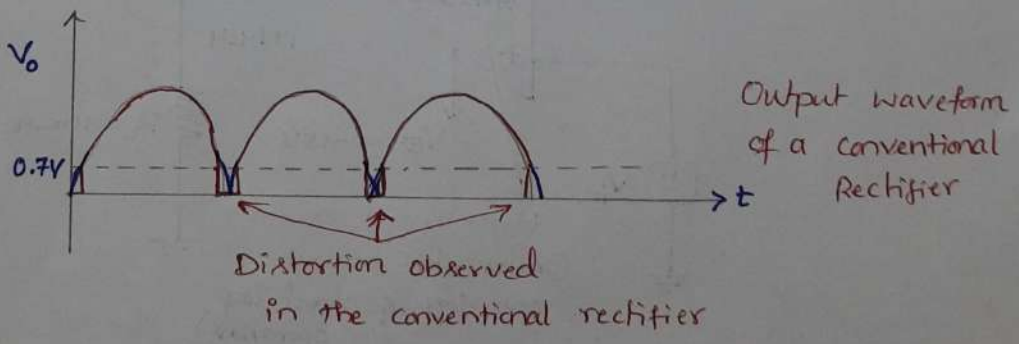
→ Limitation:- The rectifier circuit built with normal diodes cannot rectify ac voltage below 0.7V, since the cut-in voltage of the diode is 0.7V(V_{th})

- The input signal has to rise to a cut-in voltage (V_{th}) before appreciable change can be seen at the output.

- For $V_{in} > V_{th}$, $V_o = V_{in} - V_{th}$

  For $V_{in} < V_{th}$, $V_o = 0V$

- Due to this, the output of a conventional rectifier is distorted



→ To achieve precision rectification, we need a circuit that keeps $V_o = V_{in}$ for $V_{in} > 0$

→ This can be achieved by using op-amp along with the diodes and these circuits are called Precision rectifiers

Definition: Precision rectifiers are the circuits used to rectify voltages having amplitudes less than 0.7V. Hence, these circuits are called Small Signal Precision Rectifiers

Precision Half-Wave Rectifiers

The precision half-wave rectifiers are classified as

1. Positive Half-wave Rectifier
2. Negative Half-wave Rectifier

1. Positive Small-signal Half-wave Rectifier

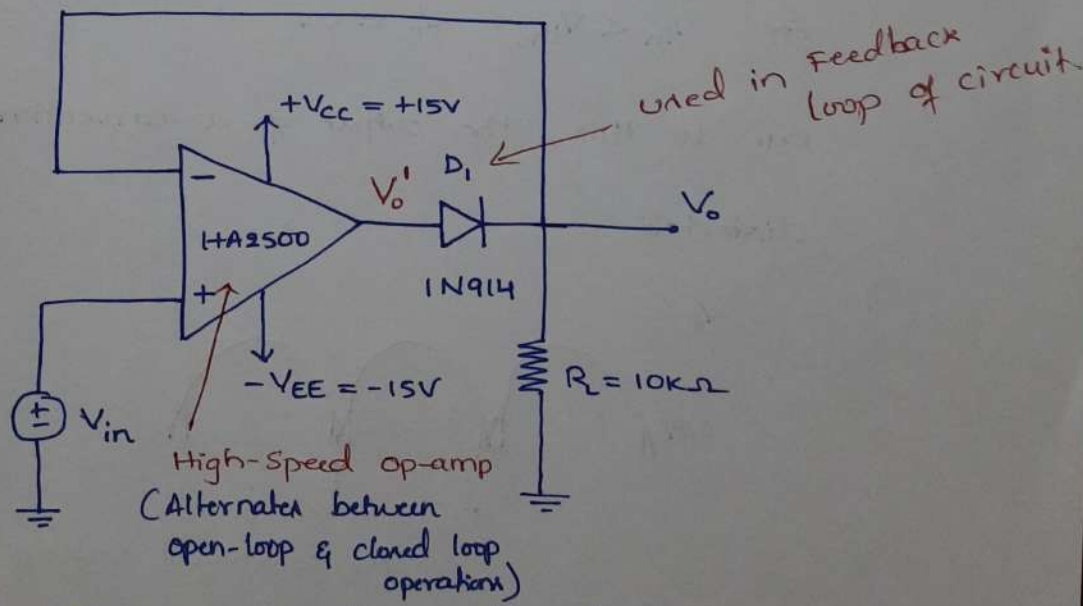


Fig. 1. Positive Small Signal Half-wave Rectifier circuit

→ Fig. 1. shows positive small signal half-wave rectifier circuit.

→ The resultant circuit rectifies signals with peak values down to a few mV unlike conventional diodes.

→ High open-loop gain of the op-amp automatically adjusts the voltage drive to the diode D_1 so that the rectified output peak is same as the input.

→ The diode acts as an ideal diode (switch) since the voltage drop across the ON diode is divided by the open-loop gain of the op-amp.

→ The circuit analysis can be done for

$$V_{in} > 0 \quad \text{and} \quad V_{in} < 0$$

Case (i): $V_{in} > 0$

→ As V_{in} starts increasing in the positive direction, V_o' also starts increasing positively until diode D_1 is forward biased

→ Due to high open-loop gain of op-amp, it produces high V_o'. This provides enough drive to diode D_1 to make it forward biased.

→ Since the diode acts as ideal diode, forward biased ~~bias~~ diode behaves as a closed switch.

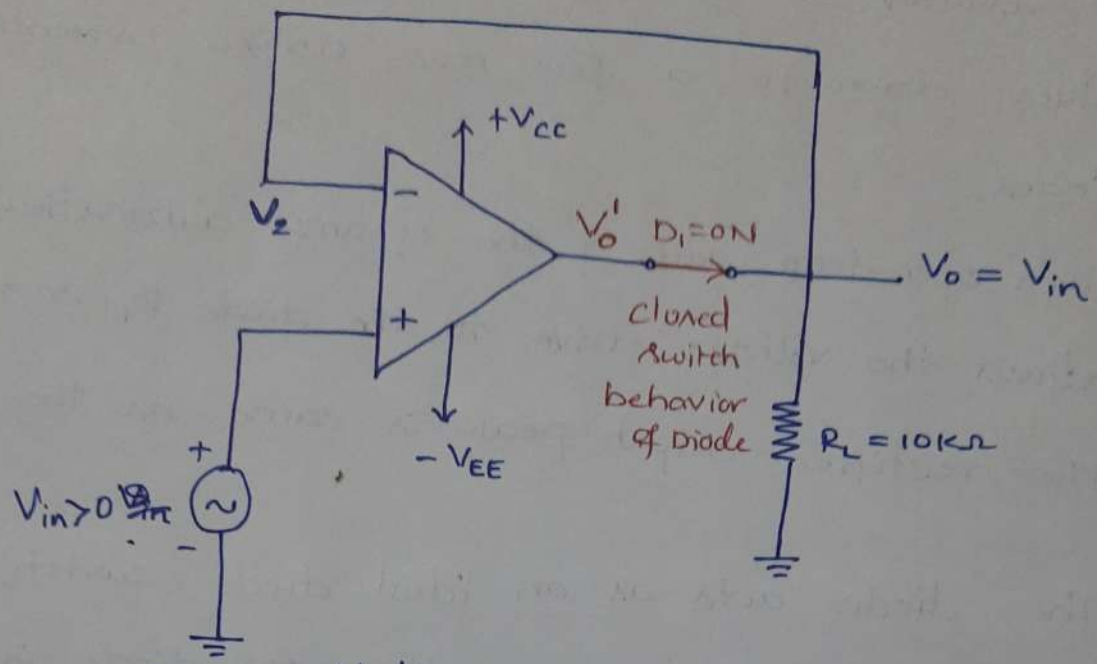


Fig. 2. Half-wave Rectifier for $V_{in} > 0$

→ The cutin voltage of a diode of 0.7V gets divided by A_{OL} which is very high. Hence immediately as V_{in} starts increasing D_1 becomes ON.

→ The circuit works as a voltage follower

→ From virtual ground: $V_2 = V_{in}$

$$\Rightarrow \boxed{V_o = V_{in}}$$

→ Hence entire positive ~~cycle~~ half cycle is available across the load.

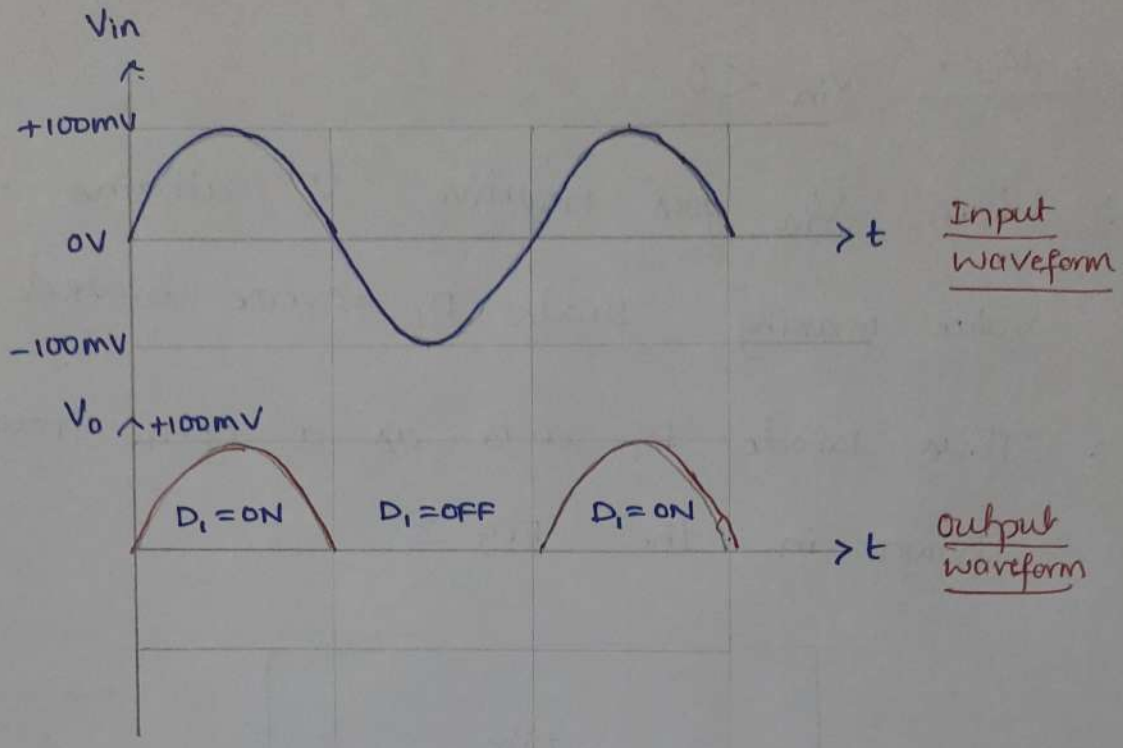


Fig. 4. Input- output waveform : Positive Small Signal Half- Wave Rectifier

→ Thus, compared to conventional rectifiers, precision rectifiers can rectify very small voltages of the order of few milli volts

→ For the positive input cycle, the positive output cycle exists at the output, hence the circuit is also called non-inverting half-wave precision rectifier.

2. Negative Half-Wave Rectifier

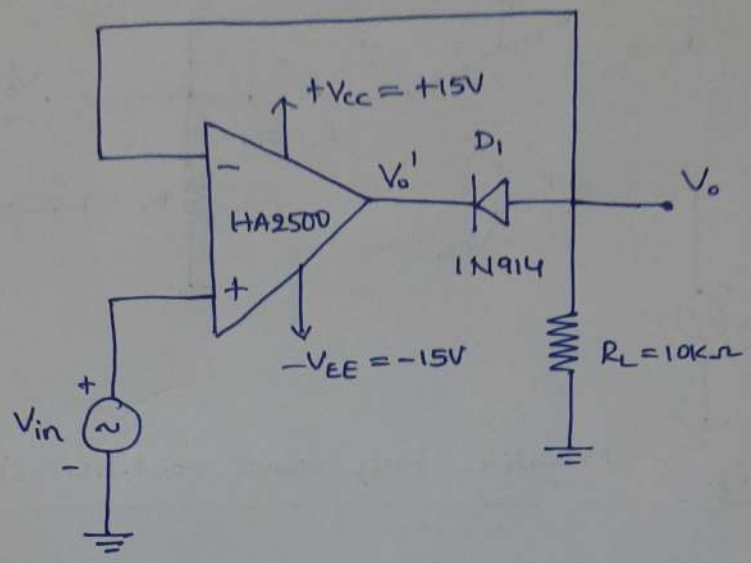


Fig. 5. Negative small signal Half-wave Rectifier circuit

→ Fig. 5 shows negative small signal half-wave rectifier circuit.

→ By changing the direction of diode D_1 in positive half-wave rectifier circuit, the negative half-wave rectifier can be obtained.

Case (i): $V_{in} > 0$

→ when $V_{in} > 0$ i.e V_{in} starts increasing in the positive direction, V_o' increases due to high open-loop gain

→ This reverse biases the diode, making it open. Thus, $V_o = 0$ as no current flows through R_L

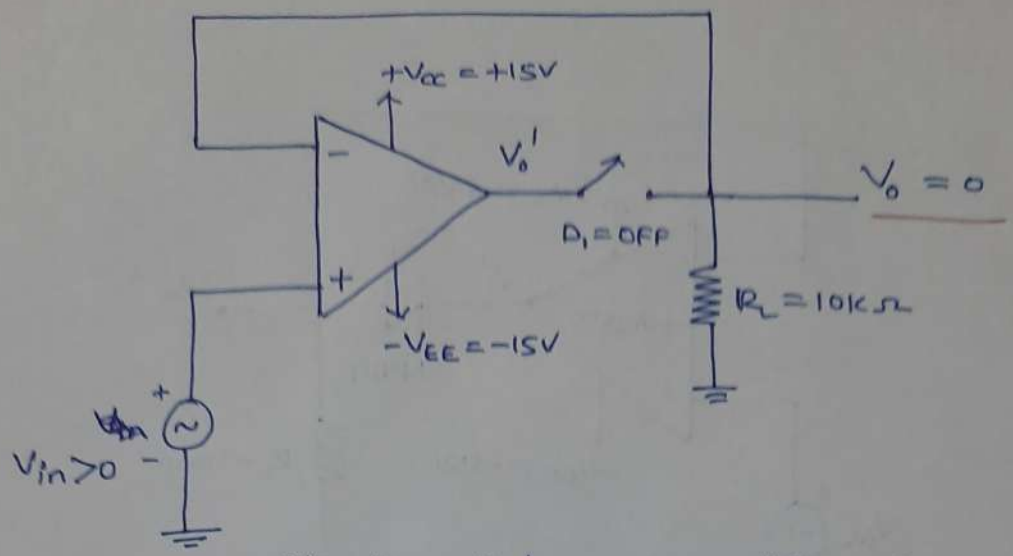


Fig. 6 Negative Half-wave rectifier circuit for $V_{in} > 0$

Case (ii): $V_{in} < 0$

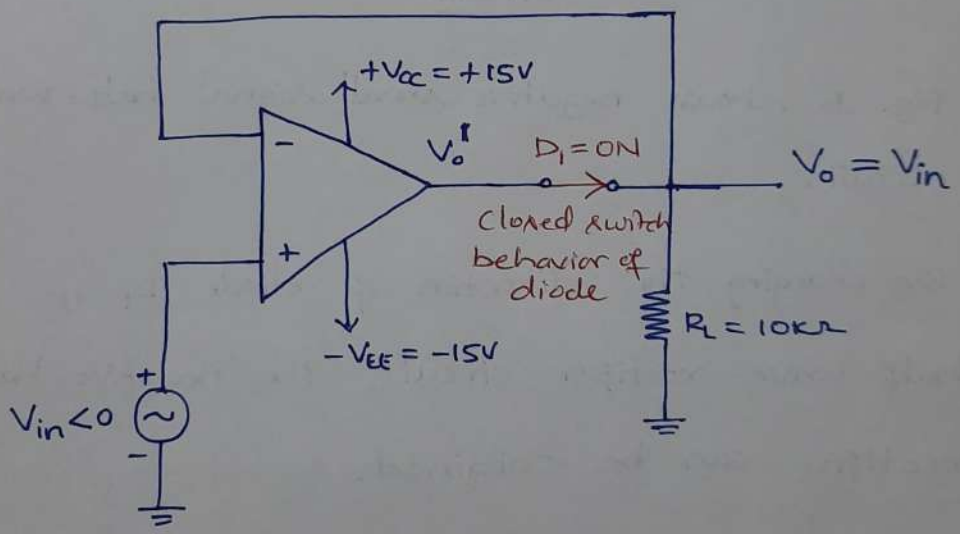


Fig. 7. Negative Half-wave Rectifier circuit for $V_{in} < 0$

→ When $V_{in} < 0$ i.e negative going input signal, V_0' decreases. Since V_0' is highly negative which forward biases the diode D_1 making it ON.

→ The diode acts as a short-circuit and the circuit behaves as a voltage follower.

→ Hence, the output voltage is same as the input voltage.

→ Thus the entire negative half cycle is available across the load.

→ Hence, the circuit is called negative half-wave rectifier.

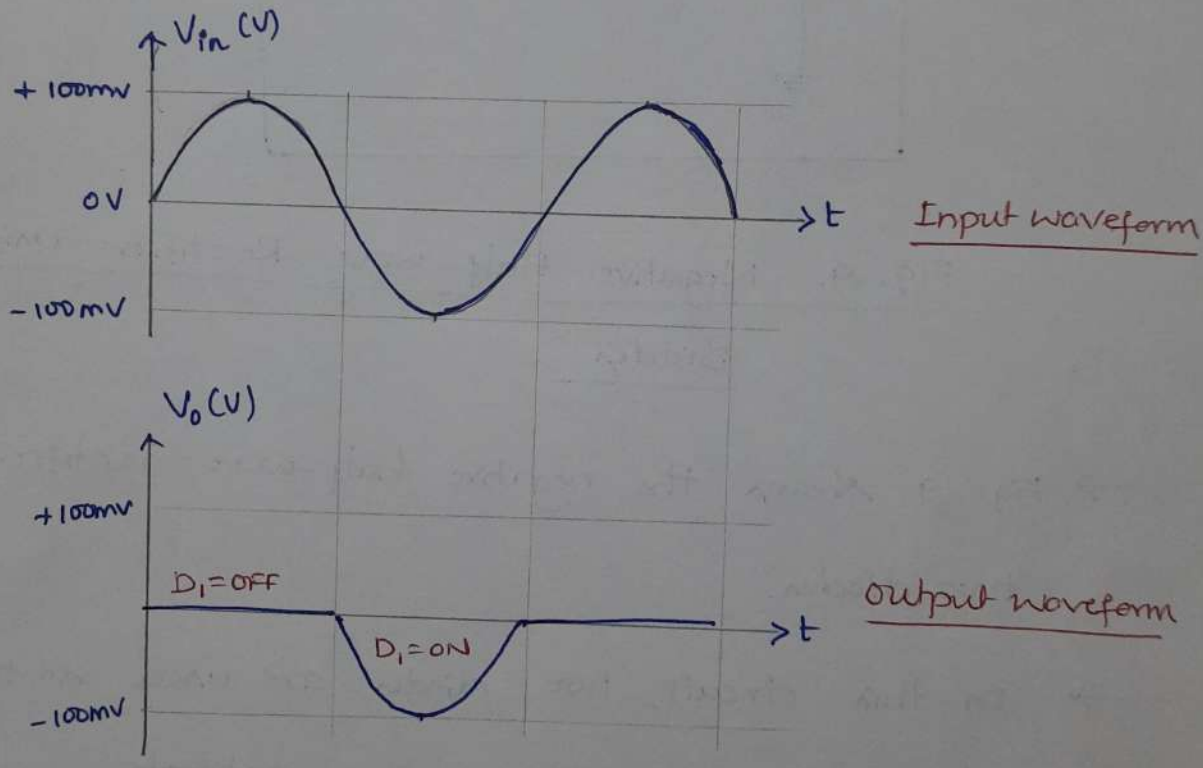


Fig. 8. Input-Output Waveform: Negative Small Signal Half-Wave Rectifier

Negative Half-wave Rectifier using Two Diodes

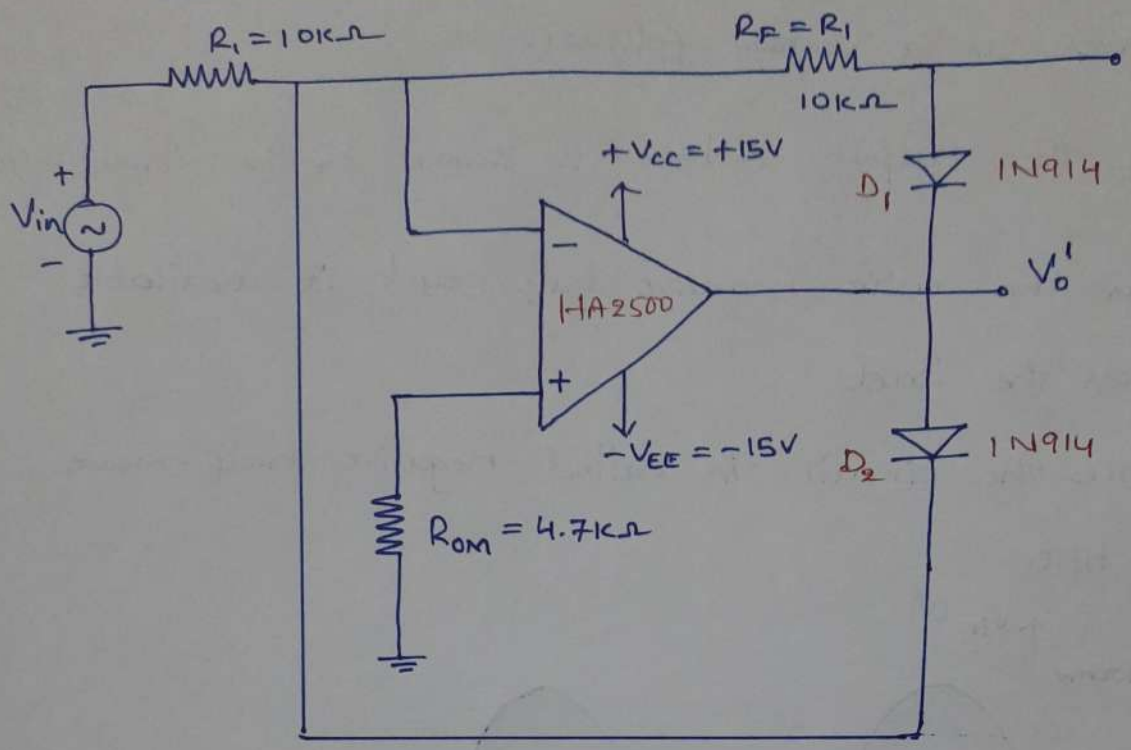


Fig. 9. Negative Half-wave Rectifier using two Diodes

→ Fig. 9 shows the negative half-wave rectifier using two diodes.

→ In this circuit, two diodes are used so that output V_o' of an op-amp does not saturate.

→ Minimizes response time and increases the operating freq. range of an op-amp.

→ Op-amp is used in inverting configuration and output is measured at the anode of diode D_1 with respect to ground.

→ Also, the output resistance is non-uniform since it depends on the state of the diode, D_1

In otherwords: D_1 = ON, Output Impedance = low

D_1 = OFF, Output Impedance = High

→ This problem, however can be cured by connecting a voltage follower stage at the output.

Case (i): $V_{in} > 0$

Op-amp output goes negative

D_1 = Forward Biased

D_2 = Reverse Biased

Feedback loop, R_F is closed.

$$V_o = -\frac{R_F}{R_1} V_{in} = -V_{in}$$

$$\boxed{V_o = -V_{in}}$$

Case (ii): $V_{in} < 0$

Op-amp output goes positive

D_1 = Reverse Biased

D_2 = Forward Biased

~~$V_o = -(-V_{in})$~~ $V_o = 0$ since D_2 = OFF

→ To obtain positive half-wave rectified output, D_1 & D_2 must be reversed

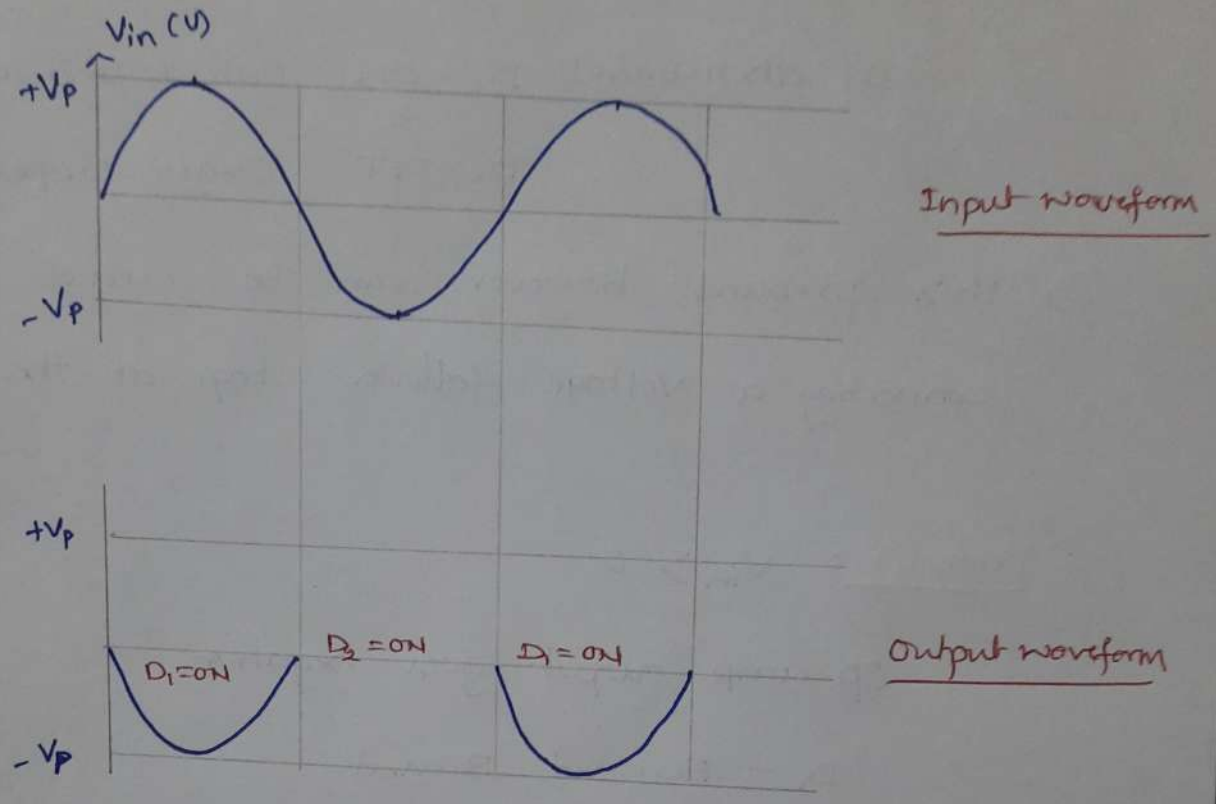


Fig. Input-Output Waveform : Negative Half-wave Rectifier using two diodes

Introduction Active Filters

Defn: An electric filter is a freq. selective ckt that pass specified band of frequencies and blocks or attenuate signals of frequencies outside this band

* **Types of Filters:**

Filters may be classified in a number of ways:

1. Analog or Digital
2. Passive or active
3. Audio or radio frequency (RF) (AF)

1. Analog or Digital Filters

* **Analog Filters:** These filters are designed to process analog signals
* **Digital Filters:** Digital filters process analog using digital techniques

2. **Passive or Active Filters:** Depending on the type of elements used in the construction, filters may be classified as ~~as~~ passive or active filters

* **Passive Filters:** Resistors, Capacitors and Inductors are used in passive filters
* **Active filters:** Transistors or op-amps with resistors and capacitors are employed in the construction of active filters.

Type of elements used ⟶ Dictates operating freq. range of filter

① RC Filters: used for audio or low freq. operation

② LC Filters / crystal Filters: used at RF and or high frequencies.

→ Crystals provide more stable operation at higher frequencies

→ This chapter presents analysis and design of analog active-RC (audio-freq) filters using op-amps.

→ Inductors are not used in audio freq. range

Because: → Very large (Size of Inductors)
→ Costly
→ Dissipate more power
→ emit magnetic fields.

Advantages of Active Filters

An active filters offer the following advantages over a passive filter:

1. Reduced size and weight: All elements with op-amp are used in Integrated circuit (IC) form.
2. Low cost (due to availability in IC form) ⇒ More economical Bec. of the absence of Inductors in active filters
3. less attenuation: Gain can be controlled in the closed loop fashion.
4. Freq. adjustment flexibility: easier to tune and adjust
5. No loading problems: Bec. op-amps used in active filter have: $Z_{in} = \infty$, $Z_o = 0$
6. Realized under class of functions: Butterworth, Thomson, chebyshev, & Cauer.

7. Improved response compared to passive filters (due to high quality components)

8. Design procedure is simple

9. More gain, less attenuation

Disadvantages of Active Filters

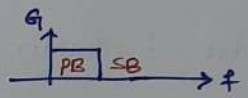
1. Finite Bandwidth of the active devices : Limits high freq. operation

2. High Sensitivity : active components are sensitive to temperature and environmental changes

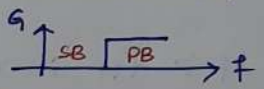
3. Requires dc power supply

The commonly used Filters are

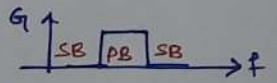
1. Low-pass filter.



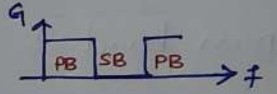
2. High-pass filter.



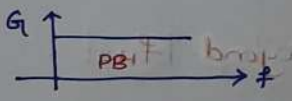
3. Band-pass filter



4. Band-reject filter



5. All pass filter



→ Active Filters are extensively used in the field of communication and signal processing

Ex: Radio, Television, Telephone, radar, Space satellites, Bio-medical equipments, etc.

→ Active Filter uses : Active element : Op-amp

passive element : Resistors and Capacitors.

Op-amp: UA741 : Works satisfactorily in active filter

But

High Speed op-amps : LM318 or ICL8017 Improve filter performance
- High slew-rate
- High unity-gain Bandwidth

⊛ Frequency Response characteristics of Active Filter

Note: Dashed curve represent : Ideal Response

Solid lines represent : Practical Filter Response

1. Low-pass Filter

→ 0 Hz to f_H (High cut-off frequency) : Constant gain

Bandwidth = f_H

→ At f_H : Gain drops by 3 dB

→ For $f > f_H$: Gain decreases with the increase in input frequency.

	Freq. Range
pass-band :	0 to f_H
Stop-band :	Beyond f_H

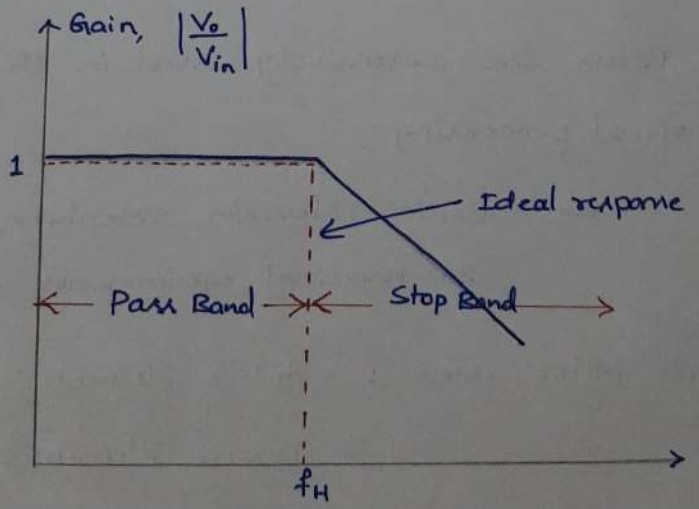


Fig. 1 Freq. Response of Low-pass Filter

→ Fig. 1 shows the freq. response of the low-pass filter

→ Ideal filter has : zero loss : Pass-band

Infinite loss : Stop-band

→ Ideal filter response ≠ Practical response

Bec. of discontinuities are not produced by linear networks

→ use of: ① proper design techniques
② precision components
③ High-Speed op-amps
⟹ Practical response ≅ Ideal response

→ ① Butterworth, ② Chebyshev, and ③ Cauer filters are commonly used practical filters that approximate the ideal response.

① Butterworth Filter: Flat pass-band and Stop-band

⟹ Butterworth filter is sometimes called as "simple design" flat-flat filter

② Chebyshev Filter: Pass-band : Ripple
Stop-band : Flat

③ Cauer Filter: Pass-band : Ripple
Stop-band : Ripple

2. High-Pass Filter

Pass-band : $f > f_L$

Stop-band : $0 < f < f_L$

f_L = low cut-off frequency

f = Operating frequency

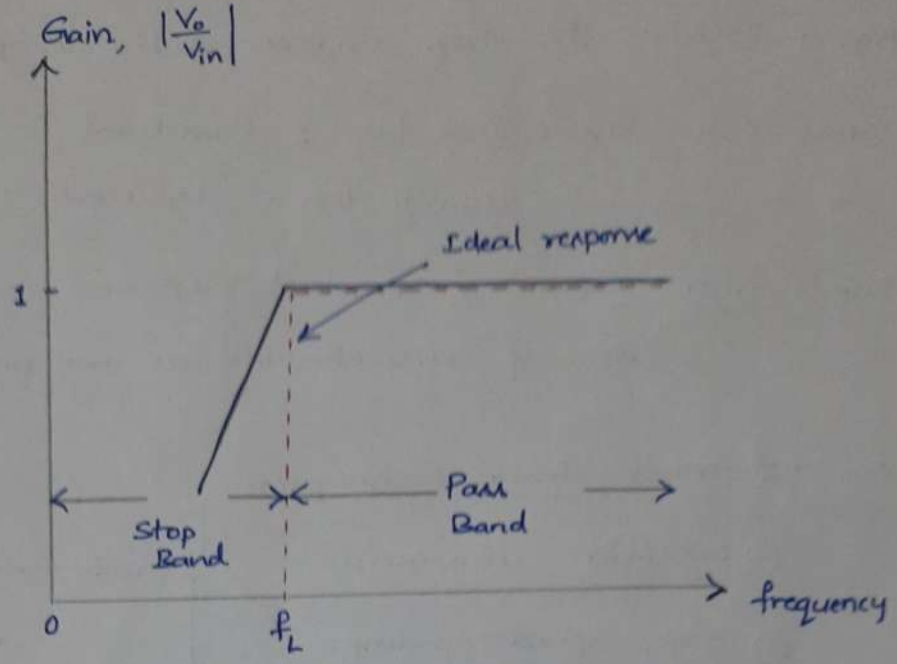


Fig. 2. Frequency Response of High-Pass Filter

3. Band-pass Filter : Fig. 3 shows the freq. response of a Band-pass filter.

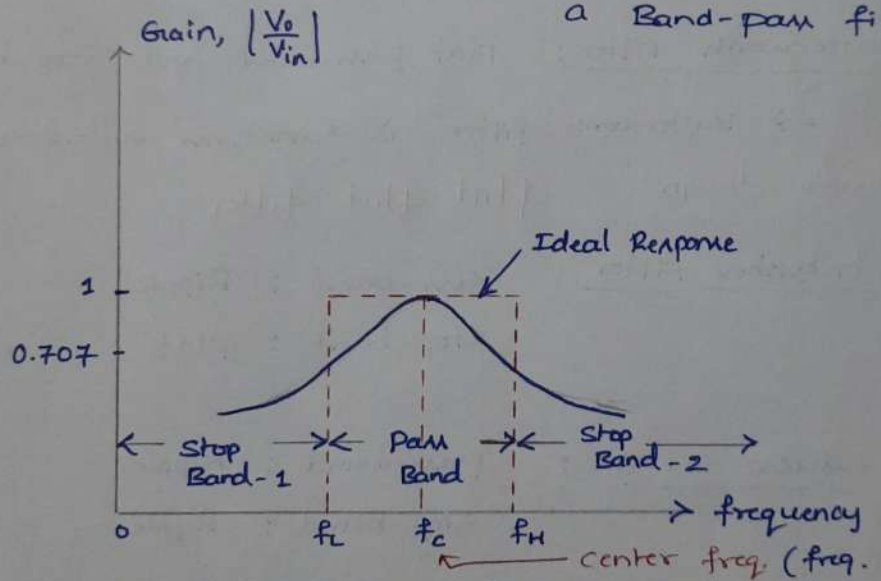


Fig. 3. Frequency Response of Band-pass Filter

Pass-band : Between cutoff frequencies f_H and f_L where $f_H > f_L$

Two stop-bands : Stop-band-1 : $0 < f < f_L$, and

Stop-band-2 : $f > f_H$

Bandwidth = $f_H - f_L$

H. Band-reject Filter

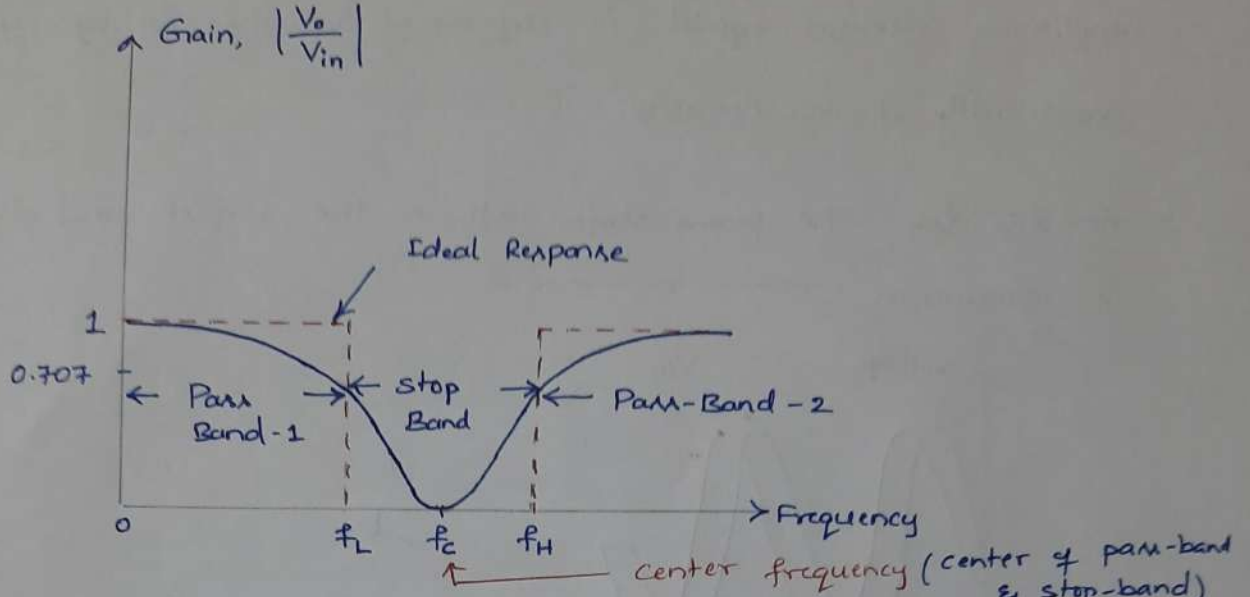


Fig. H. Frequency Response of Band-reject Filter

→ Fig. H. shows, the frequency response of a Band-reject Filter

→ The Band-reject filter performs exactly opposite to the Band-pass filter.

Stop-Band : Between two cut-off frequencies f_H and f_L

Two pass Bands : Pass-band-1 : $0 < f < f_L$, and

Pass-band-2 : $f > f_H$

→ The Band-reject filter is also called a Band-Stop or Band-elimination Filter

5. All-pass Filter

→ Fig. 5. shows the phase-shift between input and output voltages of an all-pass filter.

→ All-pass filter passes all frequencies equally well i.e output and input voltages are equal in amplitude for all frequencies with the phase shift existing b/w them.

→ The highest frequency upto which the input and output amplitudes remain equal is dependent on the unity-gain bandwidth of an op-amp.

→ At this freq. the phase-shift between the input and output is maximum.

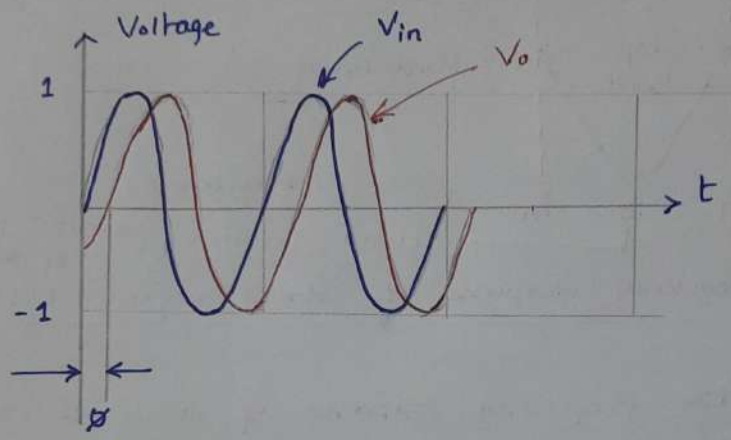


Fig. 5. phase shift between Input and Output Voltages of an All-pass Filter

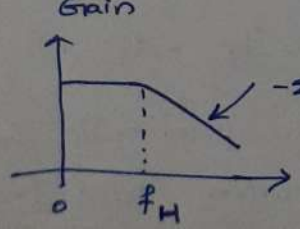
⑧ Reexamine Filter characteristics

→ Actual response curves of the filter in stop band: steadily ↑ or ↓ or both with frequency

→ Order of the Filter: The rate at which gain of the filter changes in the stop-band is determined by the order of the filter.

Example: First order Low pass filter

Gain rolls off at 20 dB/decade in stop-band for $f > f_H$



Example : 2

Second order filter low-pass filter

Roll-off rate = -40 dB/decade

Example : 3

First order high-pass

Roll-off rate : $+20$ dB/decade until $f = f_L$

Example : 4

Second order high-pass filter

Roll-off rate : $+40$ dB/decade until $f = f_L$

7.3 First order Low-pass Butterworth Filter

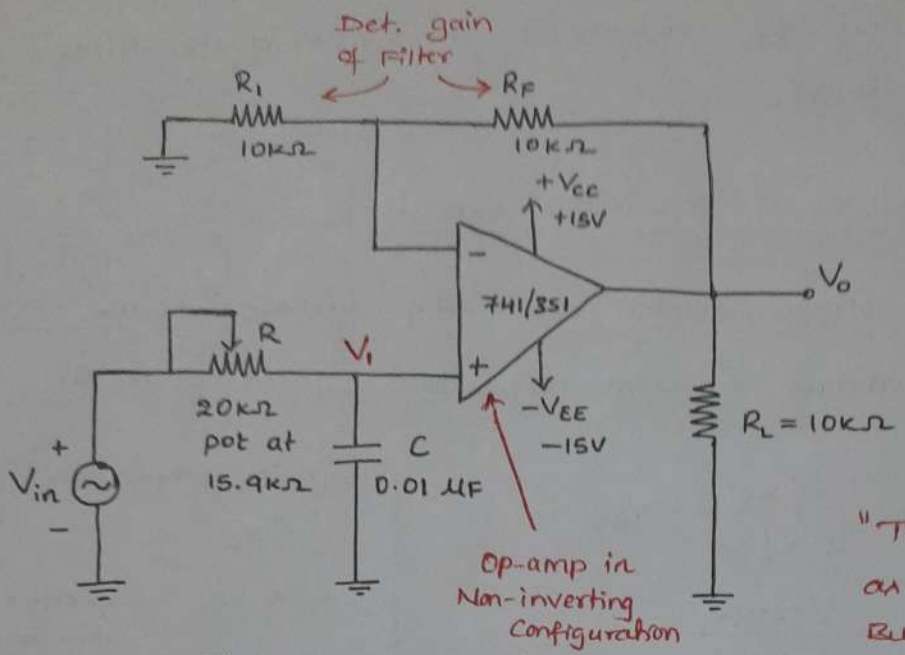


Fig. 6. First order low-pass Butterworth Filter circuit

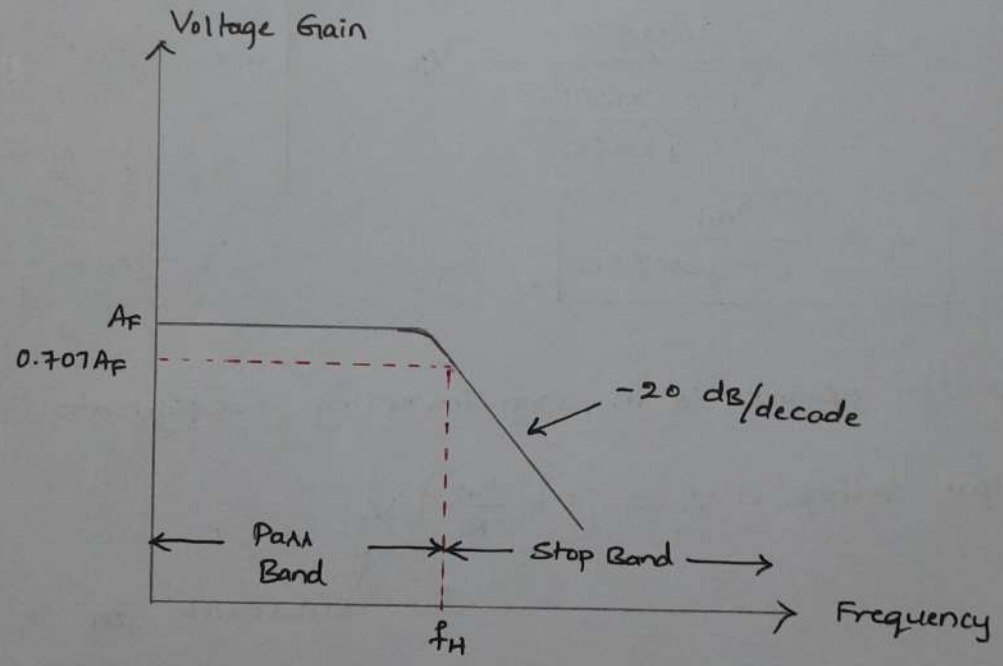


Fig. 7. Frequency Response

→ Fig. 6 shows a first order low-pass Butterworth filter that uses an RC network for filtering

→ Op-amp is used in non-inverting mode, hence it does not

load RC network.

→ Resistors R_1 and R_F determine the gain of the filter, in the pass-band.

Analysis of the Filter circuit

According to Voltage-divider rule, the voltage at the non-inverting terminal (across capacitor C) is given by

$$V_1 = \frac{-jX_c}{R - jX_c} V_{in}$$

$$V_1 = \frac{1/j2\pi fC}{R + \frac{1}{j2\pi fC}} V_{in}$$

$$V_1 = \frac{1/j2\pi fC}{\frac{1 + j2\pi fRC}{j2\pi fC}} V_{in}$$

$$\boxed{V_1 = \frac{V_{in}}{1 + j2\pi fRC}} \quad \text{—— (1)}$$

Capacitor Impedance = $-jX_c$

where X_c = Capacitive reactance

$$X_c = \frac{1}{2\pi fC}$$

$$\therefore -jX_c = \frac{-j}{2\pi fC}$$

$$-j = \frac{1}{j} \text{ or } -\frac{1}{j} = j$$

$$\therefore -jX_c = \frac{1}{j2\pi fC}$$

As the op-amp is in non-inverting configuration

Output Voltage = $V_o = \left(1 + \frac{R_F}{R_1}\right) V_1$

↑ Substitute for V_1 from Eqn. (1)

$$V_o = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{V_{in}}{1 + j2\pi fRC}\right)$$

$$\boxed{\frac{V_o}{V_{in}} = \frac{\left(1 + \frac{R_F}{R_1}\right)}{\left(1 + j2\pi fRC\right)} = \frac{A_F}{1 + j\left(\frac{f}{f_H}\right)}} \quad \text{—— (2)}$$

where $A_F = \left(1 + \frac{R_F}{R_1}\right)$ = Gain of filter in Pass Band.

f = Frequency of the input signal

$f_H = \frac{1}{2\pi RC}$ = High cut-off frequency of the filter

$\frac{V_o}{V_{in}}$ = Gain of the filter as a function of frequency

→ The gain magnitude and phase angle equations of the low pass filter can be obtained by converting eqn. (2) into its equivalent polar form, as follows:

$$\text{Gain Magnitude} = \left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}} \quad \text{——(3)}$$

$$\text{phase} = -\tan^{-1}\left(\frac{f}{f_H}\right) = \phi = \text{phase angle in degrees}$$

→ The operation of the low-pass filter can be verified from the gain magnitude eqn. (3)

1. At very low frequencies, i.e $f < f_H$

$$\left|\frac{V_o}{V_{in}}\right| \cong A_F$$

2. At $f = f_H$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{2}} = 0.707\,A_F$$

3. At $f > f_H$

$$\left|\frac{V_o}{V_{in}}\right| < A_F$$

→ For range of frequencies, $0 < f < f_H$, the gain is almost constant equal to f_H which is the high cutoff freq.

→ At $f = f_H$, gain reduces to 0.707 i.e 3 dB down from A_F

→ As the freq ↑ than f_H the gain decreases at the rate of 20 dB/decade

→ 20 dB/decade : Decrease in gain by 20 dB per 10 times change in freq.

→ f_H = Break freq. or cutoff freq. or Corner freq.

Active Filters Cont.,

Definitions

1. Transfer Function : T(s)

The ratio of laplace transform of output to laplace transform of input.

$$T(s) = \frac{V_o(s)}{V_{in}(s)} \quad \text{—— (1)}$$

Replacing s by jω we get the frequency domain transfer function

$$T(j\omega) = \frac{V_o(j\omega)}{V_{in}(j\omega)} \quad \text{—— (2)}$$

→ Consider the transfer function of the form given by

$$T(s) = \frac{a_1 s + a_2}{b_1 s + b_2} = \frac{N(s)}{D(s)} \quad \text{—— (3)}$$

where a_1, a_2, b_1 and b_2 are real constants; may be either positive or negative

Then eqn. (3) can be modified as

$$T(s) = \frac{a_1}{b_1} \cdot \frac{s + \left(\frac{a_2}{a_1}\right)}{s + \left(\frac{b_2}{b_1}\right)} = K \frac{s + z_1}{s + p_1} \quad \text{—— (4)}$$

↑ System gain factor or scale factor

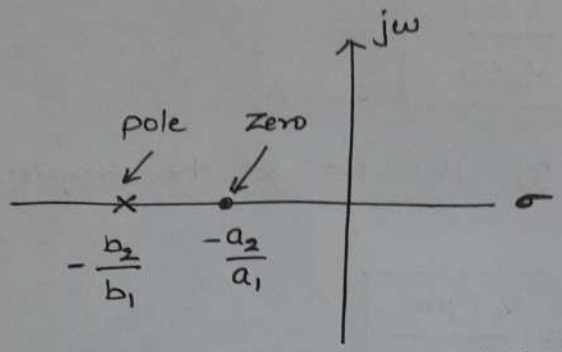
→ The complex frequencies which make the value of the system function infinite are called poles.

From eqn. (4) $s = -p_1$ is the pole of the system

The system function becomes infinite when we substitute $s = -p_1$ in eqn. (4)

→ The complex frequencies which make the value of the system function zero are called zeros.

From eqn. (4) $s = -z_1$ is the zero of the system. The system function becomes zero when we substitute $s = -z_1$ in eqn. (4)



Note: Pole-zero plot doesn't show K

Fig. 1. pole zero plot of a Transfer Function

2. Pass-Band:

The band of frequencies for which the gain of the filter remains constant. i.e it allows to pass the frequencies is called pass-band of the filter.

3. Stop-Band:

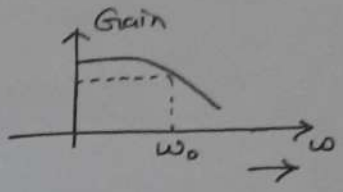
The band of frequencies for which the gain of filter becomes almost zero i.e it stops the frequencies to pass is called stop-band. of the filter.

4. Attenuation: Practically gain starts decreasing from a particular frequency and becomes zero after certain band of frequencies. This band is called transition band.

and decrease in gain in this transition band is called attenuation.

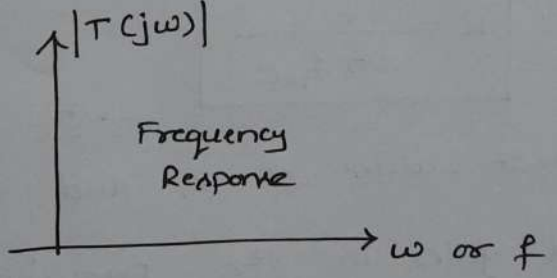
5. cut-off Frequency:

The frequency of the filter where the filter changes its function is called its cut off frequency.



6. Frequency Response:

The graph of the magnitude of the transfer function $|T(j\omega)|$ against the frequency ω is called the frequency response of the filter.



7.3.1 Filter Design

A low-pass filter can be designed by implementing the following steps:

1. Choose a value of high cutoff frequency f_H
2. Select a value of capacitance, $C \leq 1\ \mu F$

   → choose Mylar or tantalum capacitors for better performance.

   <0.001 and 1 μF Range Selection>
3. Calculate the value of R using

$$R = \frac{1}{2\pi f_H C} \quad \text{—— (5)}$$

4. Finally, select values of R_1 and R_F depending on the required gain in the pass-band.

$$A_F = \frac{V_o}{V_{in}} = 1 + \frac{R_F}{R_1} \quad \text{—— (6)}$$

7.3.2 Frequency Scaling

→ Once the filter is designed, sometimes, it is necessary to change the value of cutoff frequency f_H

→ The procedure used to convert an original cutoff frequency f_H to a new cutoff frequency f_H' is called frequency scaling <Definition>

Frequency scaling is accomplished as follows:

let original cutoff frequency = f_H
New cutoff frequency = f'_H

$$f = \frac{1}{2\pi RC}$$

$$f_H = \frac{1}{2\pi RC} \quad ; \quad f'_H = \frac{1}{2\pi R'C'}$$

$$\frac{f_H}{f'_H} = \frac{R'C'}{RC}$$

Assuming $C = C' = 0.01\,\mu F$

$$\frac{f_H}{f'_H} = \frac{R'}{R} \Rightarrow$$

New resistor, $R' = R \times \frac{f_H}{f'_H}$

f_H → original cutoff frequency

f'_H → New cutoff frequency

(P) Design a low-pass filter at a cutoff frequency of 1 KHz with a pass-band gain of 2.

Solution: Follow the preceding design steps.

1. $f_H = 1\,KHz$
2. Let $C = 0.01\,\mu F$
3. Then $R = \frac{1}{2\pi f C} = \frac{1}{(2\pi)(10^3)(10^{-8})} = 15.9\,k\Omega$

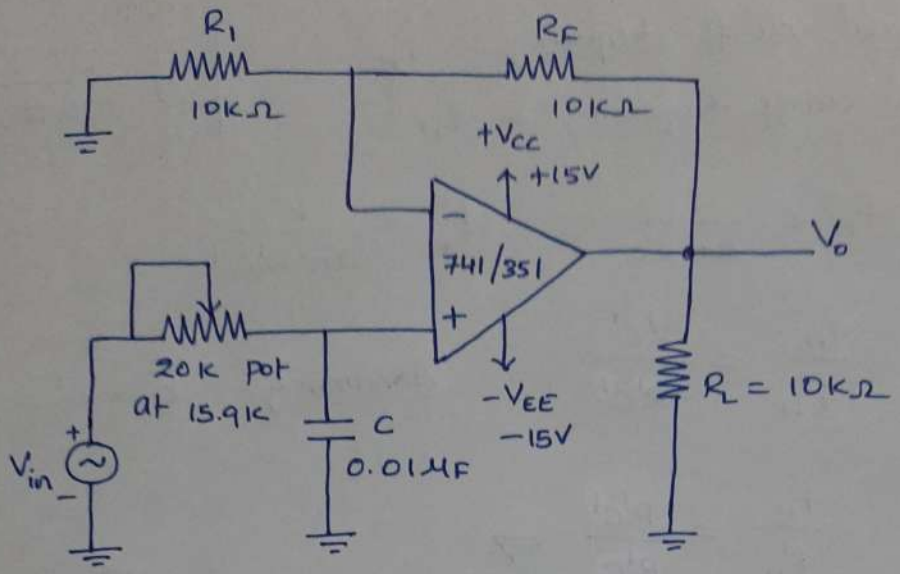
$\Rightarrow$ $\boxed{R = 15.9\ k\Omega}$ Use a 20 $k\Omega$ potentiometer

4. Since the pass-band gain is 2

R_1 and R_F must be equal

$\therefore R_F = R_1 = 10\,k\Omega$ (Say)

$$A_F = 1 + \frac{R_F}{R_1} \Rightarrow 1 + \frac{10k\Omega}{10k^2} = 2$$



Circuit Diagram: First order Low-pass Butterworth Filter

(P) Using the frequency scaling technique, convert the 1KHz cutoff frequency of the low-pass filter previous example to a cutoff frequency of 1.6 KHz.

Solution:

To change a cutoff frequency from 1KHz to 1.6KHz we multiply the 15.9KΩ resistor by

$$\frac{f_H}{f_H'} = \frac{\text{original cutoff frequency}}{\text{new cutoff frequency}} = \frac{1KHz}{1.6KHz} = 0.625$$

Therefore, new resistor, $R' = R \times \frac{f_H}{f_H'} = 15.9K \times 0.625$

$$\boxed{R' = 9.94\,K\Omega}$$

However, 9.94KΩ is not a standard value

Therefore, use R = 10KΩ potentiometer and adjust it to 9.94KΩ

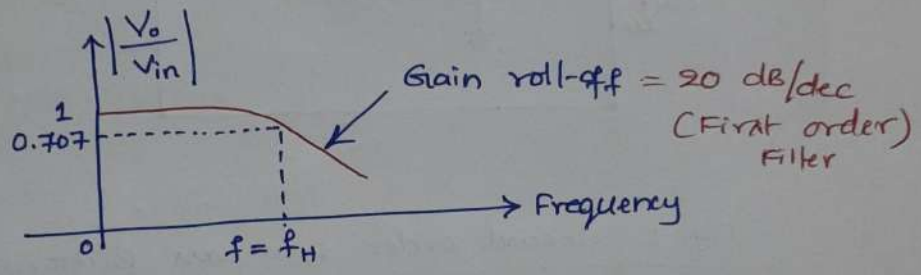
Thus the new cutoff frequency is

$$f_H = \frac{1}{(2\pi)(0.01\,\mu F)(9.94\,k\Omega)} = 1.6\,kHz$$

$$\boxed{f_H = 1.6\,kHz}$$

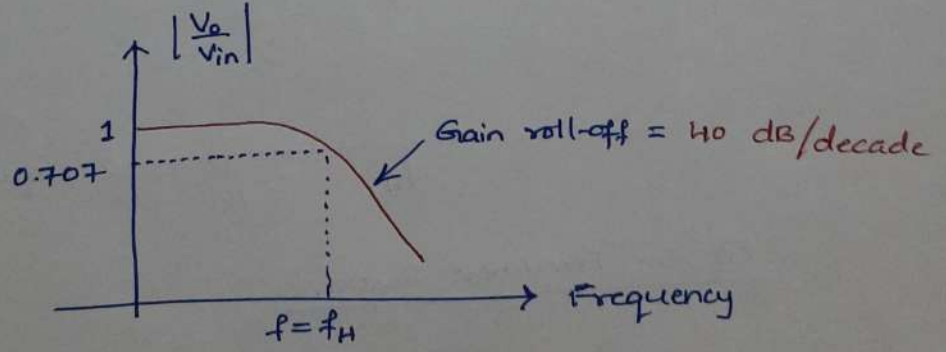
7.4 Second order Low-pass Butterworth Filter

→ In case of low-pass filter, it is always desirable that the gain rolls off very fast after the cutoff frequency, in the stop-band



In case of first order filter, it rolls off at a rate of 20 dB/decade.

→ In case of second order filter, the gain roll-off at a rate of 40 dB/decade



→ The slope of the frequency response after $f = f_H$ is −40 dB/decade

→ A first order filter can be converted to second order type by using an additional RC network as shown in Fig. 1.

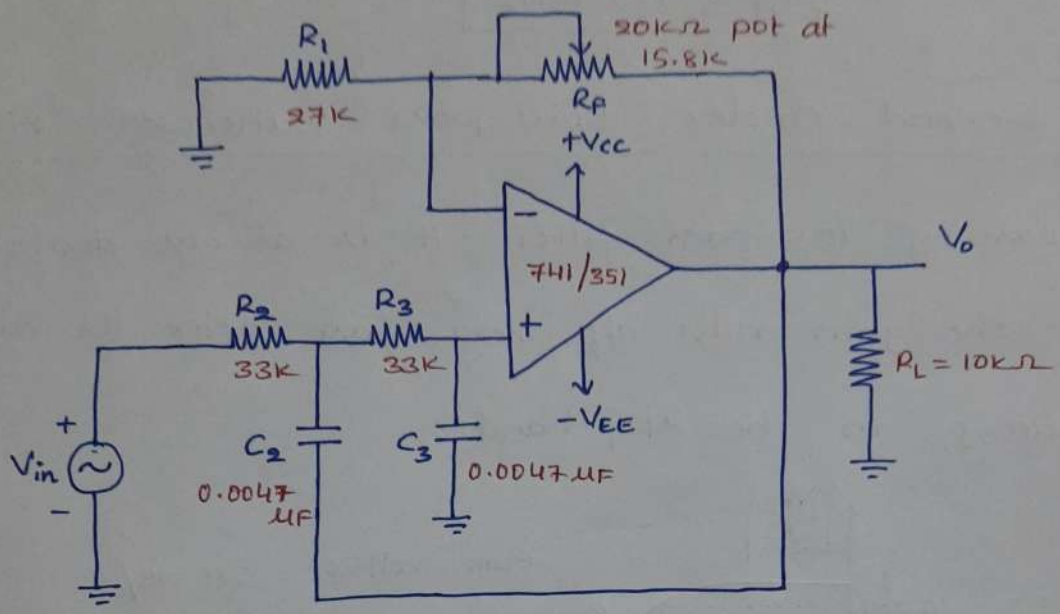


Fig. 1. Second order Low-pass Butterworth Filter circuit

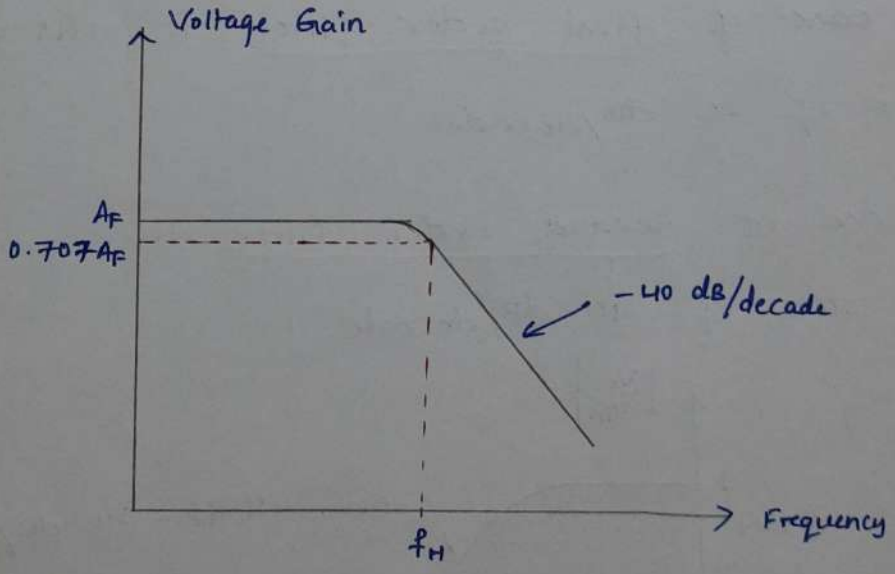
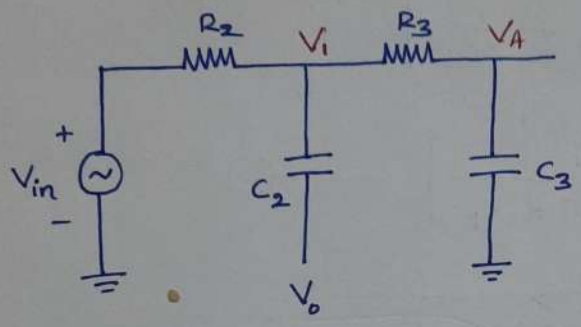


Fig. 2. Frequency Response

→ The cutoff frequency f_H for the second order Butterworth filter is decided by R_2, C_2, R_3 and C_3 as follows:

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}} \quad \text{——(7)}$$

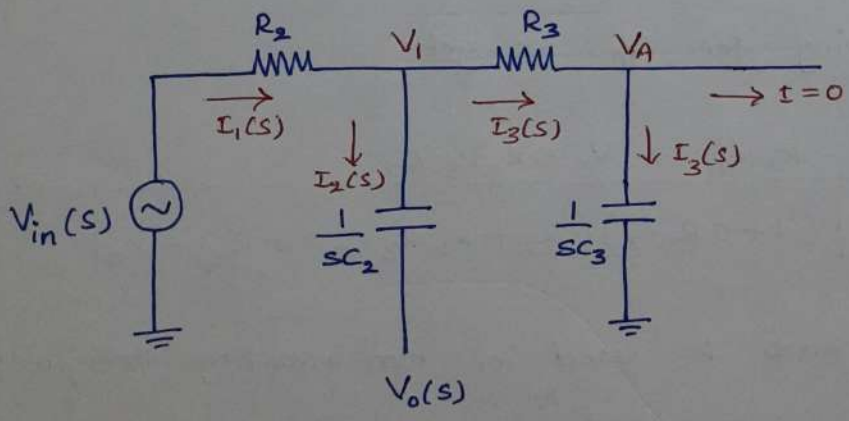
Analysis of the Filter circuit



Consider the RC network from the second-order low-pass Butterworth Filter shown in Fig. 1

Fig. 3 RC Network of Second Order Butterworth Filter circuit

The input RC network can be represented in Laplace domain as shown in Fig. 4.



$$I_1(s) = I_2(s) + I_3(s)$$

Fig. 4. RC Network of Fig. 3 Represented in Laplace Domain

Applying KCL at node V_1 we get

$$I_1 = I_2 + I_3 \quad \text{——} (8)$$

i.e $$\frac{V_{in} - V_1}{R_2} = \frac{V_1 - V_0}{\left(\frac{1}{sC_2}\right)} + \frac{V_1 - V_A}{R_3} \quad \text{——} (9)$$

using potential divider rule, we can write

$$V_A = V_1 \left[\frac{\frac{1}{sC_3}}{R_3 + \frac{1}{sC_3}} \right] \quad \text{——} (10)$$

$$V_A = V_1 \left[\frac{1}{1 + s R_3 C_3} \right] \quad \text{——} (11)$$

$$\boxed{V_1 = V_A (1 + s R_3 C_3)} \quad \text{——} (12)$$

Substituting eqn. (12) in eqn. (9) we get

$$\frac{V_{in} - V_A(1 + sR_3C_3)}{R_2} = \frac{V_A(1 + sR_3C_3) - V_0}{\left(\frac{1}{sC_2}\right)} + \frac{V_A(1 + sR_3C_3) - V_A}{R_3}$$

Solving for V_A we get

$$V_A = \frac{R_3 V_{in} + V_0 s R_2 R_3 C_2}{\left[(1 + sR_3C_3)(R_3 + R_2R_3C_2s + R_2) - R_2\right]} \quad \text{——} (13)$$

Since op-amp is used in non-inverting configuration

$$V_0 = \left(1 + \frac{R_F}{R_1}\right) V_A \overset{A_F}{\Longrightarrow} V_0 = A_F V_A$$

Therefore, $$V_0 = A_F \left[\frac{R_3 V_{in} + V_0 s R_2 R_3 C_2}{(1 + sR_3C_3)(R_3 + R_2R_3C_2s + R_2) - R_2} \right]$$

$$\frac{V_o}{V_{in}} = \frac{A_F}{s^2 + \frac{(R_3C_3 + R_2C_3 + R_2C_2 - A_F R_2C_2)s}{R_2R_3C_2C_3} + \frac{1}{R_2R_3C_2C_3}} \quad \text{—— (14)}$$

As the order of s in the gain expression is 2. The Filter is called second order filter. The system transfer function of any second order filter is given by

$$\frac{V_o(s)}{V_{in}(s)} = \frac{A}{s^2 + 2\xi\omega_n + \omega_n^2} \quad \text{—— (15)}$$

A = overall gain

ξ = Damping of a system

ω_n = Natural freq. of oscillations

$$\omega_n^2 = \frac{1}{R_2R_3C_2C_3}$$ by comparing eqn. (14) & (15)

In case of filters, this freq. is nothing but the cutoff frequency, ω_H

$$\therefore \quad \omega_H^2 = \frac{1}{R_2R_3C_2C_3} \quad \text{since } \omega_H = 2\pi f$$

$$(2\pi f_H)^2 = \frac{1}{R_2R_3C_2C_3}$$

$$\boxed{f_H = \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}} \longrightarrow \text{Cutoff Frequency}$$

—— (16)

Replacing $s = j\omega$, the transfer function can be written as

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f}{f_H}\right)^4}} \longrightarrow \text{Gain magnitude equation} \quad \text{---(17)}$$

where A_F = Gain of filter in pass Band = $1+\left(\frac{R_F}{R_1}\right)$

f = Input frequency in Hz

f_H = High cutoff frequency = $\frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$

→ The freq. response of second order Butterworth filter is shown in Fig. 2.

Frequency	Gain
0 to f_H	A_F
f_H	$0.707A_F$
$> f_H$	$< A_F$

Gain rolls off at the rate of -40 dB/decade.

7.4.1 : Filter Design

The design steps for the second order low-pass Butterworth filter are,

1. Choose the cutoff frequency, f_H
2. The design calculations can be simplified by selecting $R_2 = R_3 = R$

$C_2 = C_3 = C$

and choose a value of $C \leq 0.1\,\mu F$

3. calculate the value of R from the equation

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}} = \frac{1}{2\pi RC}$$

4. As $R_2 = R_3 = R$ and $C_2 = C_3 = C$

A_F = pass-band voltage gain $= \left(1 + \frac{R_F}{R_1}\right) = 1.586$

i.e $R_F = 0.586 R_1$

Choose $R_1 \leq 100K\Omega$ and find R_F

Note: For $R_2 = R_3 = R$

$C_2 = C_3 = C$

The transfer function takes the form

$$\frac{V_o(s)}{V_{in}(s)} = \frac{A_F}{s^2 + \frac{3-A_F}{RC}s + \frac{1}{R^2C^2}}$$

Damping factor $= \xi = \frac{3-A_F}{2}$

For second order Butterworth filter, the middle term is $\sqrt{2} = 1.414$

From normalized Butterworth polynomial

$$3 - A_F = \sqrt{2} = 1.414 \Rightarrow A_F = 1.586$$

Thus, to ensure the Butterworth response it is necessary that the gain A_F is 1.586

$$1.586 = 1 + \frac{R_F}{R_1} \quad \text{i.e} \quad \boxed{R_F = 0.586 R_1}$$

choose the value of $R_1 \leq 100K\Omega$ and find corresponding value of R_F

Note: Freq. Scaling method discussed in First order low-pass filter is applicable to second order filter.

(P) Design a second order low-pass Butterworth filter having high cutoff frequency of 1KHz. Draw its freq. response.

Solution:

Step 1: The cutoff frequency is $f_H = 1KHz$

Step 2: Choose $C_2 = C_3 = C = 0.01\,\mu F$

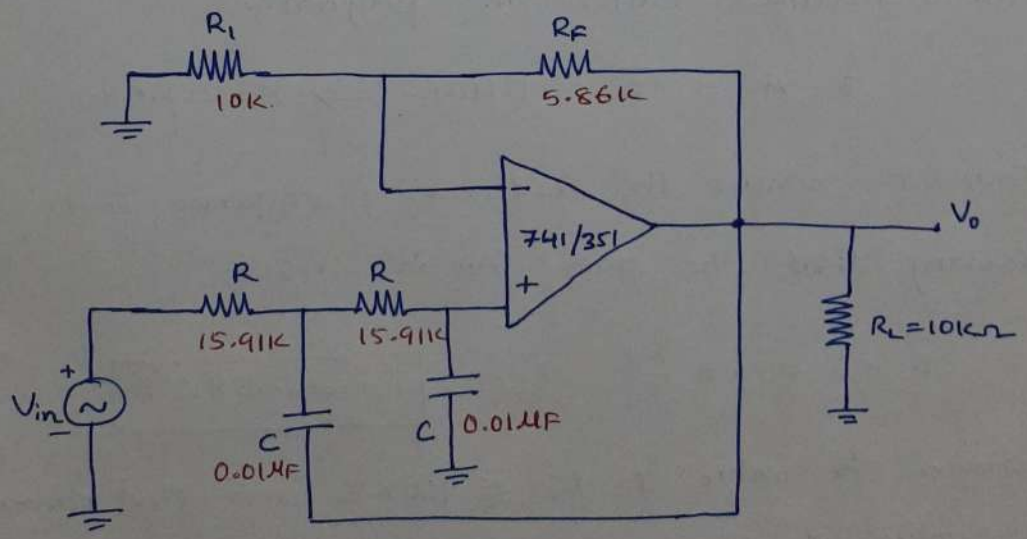
Step 3: Choose $R_2 = R_3 = R$

$$f_H = \frac{1}{2\pi RC} \quad \text{i.e} \quad 1\times10^{3} = \frac{1}{2\pi R \times 0.01\times10^{-6}}$$

$$\Rightarrow \boxed{R = 15.915\ K\Omega}$$

Step 4: $R_F = 0.586\, R_1$

Choose $\boxed{R_1 = 10K\Omega}$ hence $\boxed{R_F = 5.86K\Omega}$



The gain of the second-order filter is given by

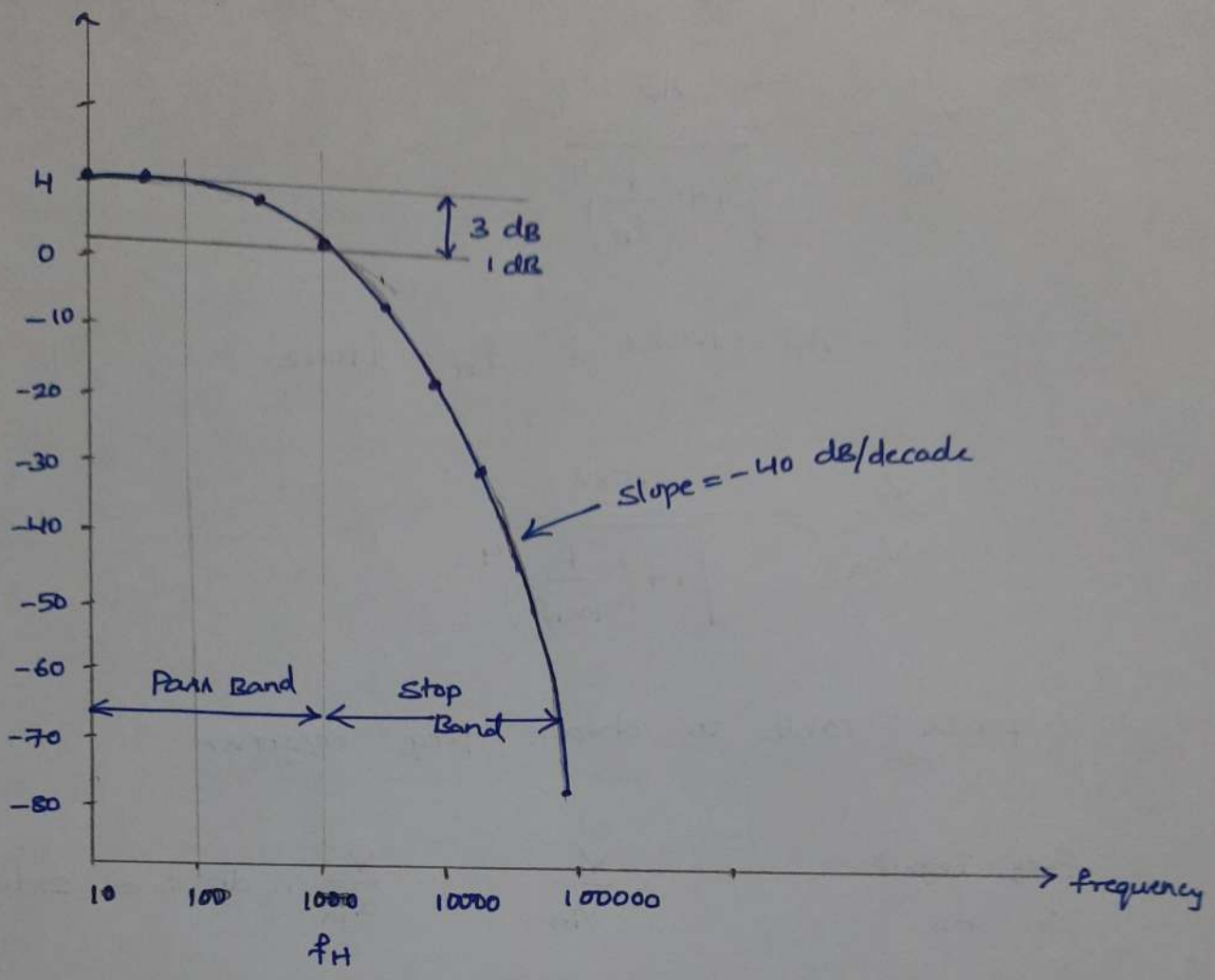
$$\frac{V_o}{V_{in}} = \frac{A_F}{\sqrt{1+\left(\frac{f}{f_H}\right)^4}}$$

$$A_F = 1.586 \; ; \quad f_H = 1\text{KHz}$$

$$\frac{V_o}{V_{in}} = \frac{1.586}{\sqrt{1+\left(\frac{f}{1\times10^3}\right)^4}}$$

preparing Table to obtain freq. response

freq. Input in Hz	$\frac{V_o}{V_{in}}$	$\frac{V_o}{V_{in}}$ in dB i.e $20\log\frac{V_o}{V_{in}}$
10	1.586	4
100	1.585	4
500	1.538	3.74
1000	1.121	1
5000	0.0633	-23.97
7000	0.032	-29.89
10000	0.015	-36.47
50000	6.34×10^{-4}	-63.95
100000	1.586×10^{-4}	-76



Frequency Response

7.5 First-Order High-Pass Butterworth Filter

Definition: A high-pass filter is a circuit that attenuates all the signals below a specified band denoted as f_L and passes frequencies above f_L

→ A high-pass filter performs the opposite function to that of low-pass filter

→ High-pass filter circuit can be obtained by interchanging frequency determining resistance and capacitance in low-pass filter circuit.

→ The first order high-pass filter can be obtained by interchanging the elements R and C in a first order low-pass filter circuit.

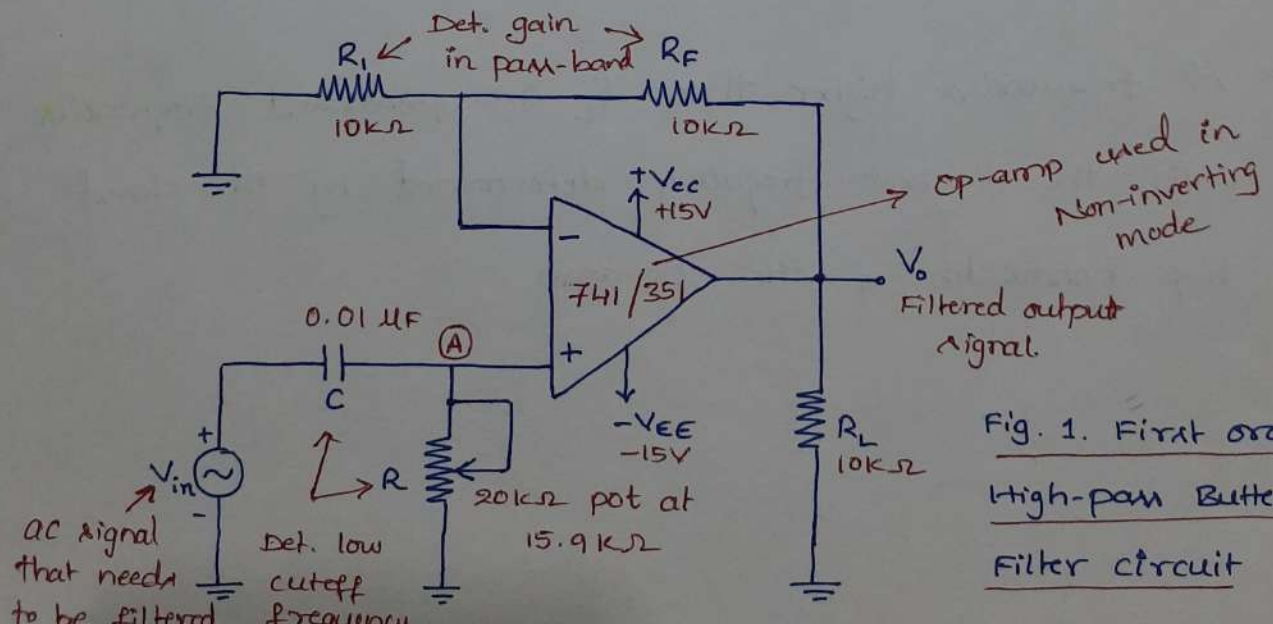


Fig. 1. First order High-pass Butterworth Filter circuit

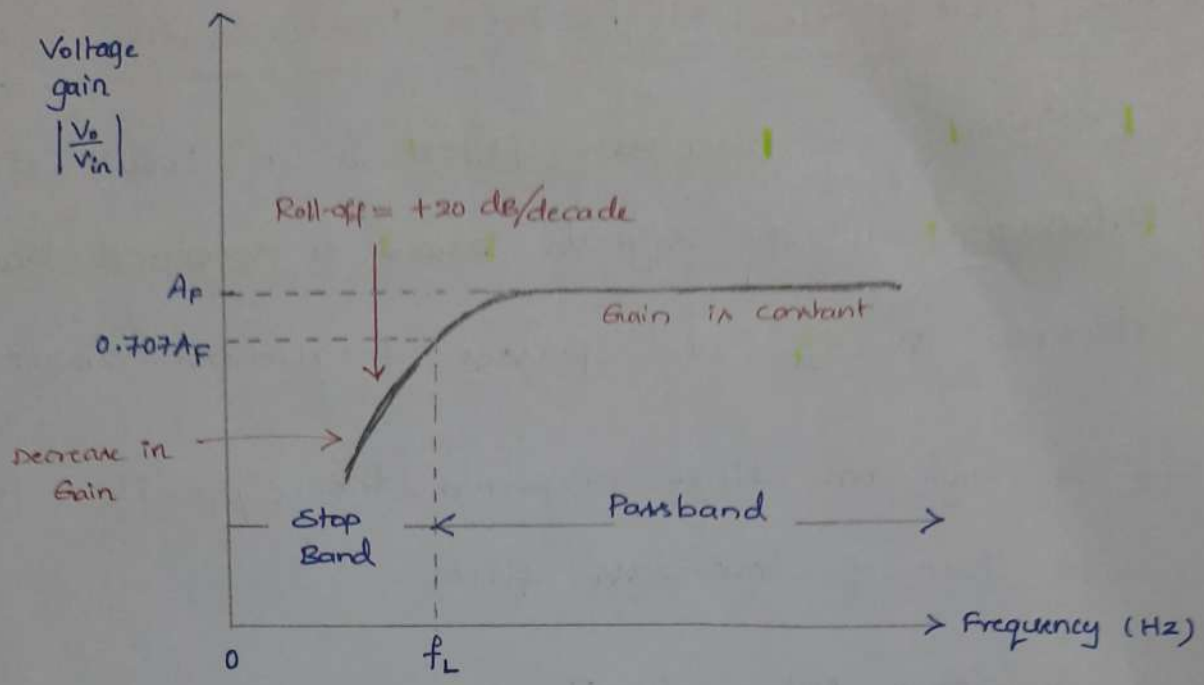


Fig. 2. Frequency Response of First-order Butterworth High-pass Filter

→ Butterworth high pass-filter of first order has low cutoff frequency of f_L. This is the frequency at which the magnitude of the gain is 0.707 times its pass-band value.

→ All frequencies higher than f_L are passband frequencies with the highest frequency determined by the closed loop bandwidth of the op-amp.

Analysis of the Filter circuit

→ The impedance of the capacitor is

$$-jX_c = -j\left(\frac{1}{2\pi fC}\right) \quad \text{——} (1)$$

where f is the input i.e operating frequency

→ Applying Voltage divider rule at Node A i.e non-inverting terminal of the op-amp

$$V_A = V_{in}\left[\frac{R}{R - jX_c}\right] \quad \text{——} (2)$$

$$V_A = V_{in}\left[\frac{R}{-jX_c\left(\frac{R}{-jX_c} + 1\right)}\right] \quad \text{——} (3)$$

Taking $-jX_c$ outside

As $-\frac{1}{j} = j$ we can write

$$\frac{1}{-jX_c} = \frac{j}{X_c} = \frac{j}{\left(\frac{1}{2\pi fC}\right)} = j2\pi fC \quad \text{——} (4)$$

$$V_A = V_{in}\left[\frac{R/-jX_c}{\left(\frac{R}{-jX_c} + 1\right)}\right] \quad \text{——} (5)$$

Substituting (4) in (5)

$$V_A = V_{in}\left[\frac{j2\pi fRC}{1 + j2\pi fRC}\right] \quad \text{——} (6)$$

Since $f_L = \frac{1}{2\pi RC}$ ⇒ Eqn. (6) changes to

↙ Low cutoff Frequency

$$V_A = V_{in}\left[\frac{j\left(\frac{f}{f_L}\right)}{1+j\left(\frac{f}{f_L}\right)}\right] \quad \text{——⑦}$$

Now, for the op-amp in non-inverting configuration

$V_o = A_F V_A$ ——⑧ where V_A = Voltage at non-inverting input

$A_F = \left(1 + \frac{R_F}{R_1}\right)$ ⇒ Gain of the op-amp in pass band

Substituting eqn. ⑦ in eqn. ⑧

$$V_o = A_F V_{in}\left[\frac{j\left(\frac{f}{f_L}\right)}{1+j\left(\frac{f}{f_L}\right)}\right]$$

$$\frac{V_o}{V_{in}} = A_F\left[\frac{j\left(\frac{f}{f_L}\right)}{1+j\left(\frac{f}{f_L}\right)}\right] \quad \text{——⑨}$$

This is the required expression for the transfer function of the filter.

→ For the freq. response, we require the magnitude of the transfer function, which is given by

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F\left(\frac{f}{f_L}\right)}{\sqrt{1+\left(\frac{f}{f_L}\right)^2}} \quad \text{——⑩}$$

Eqn. ⑩ describes the behavior of the high-pass filter

1. At low frequencies, i.e $f < f_L$,

$$\left|\frac{V_o}{V_{in}}\right| < A_F$$

$\Rightarrow$ low frequency signals are attenuated.

2. At $f = f_L$, $\left|\frac{V_o}{V_{in}}\right| = 0.707 A_F$

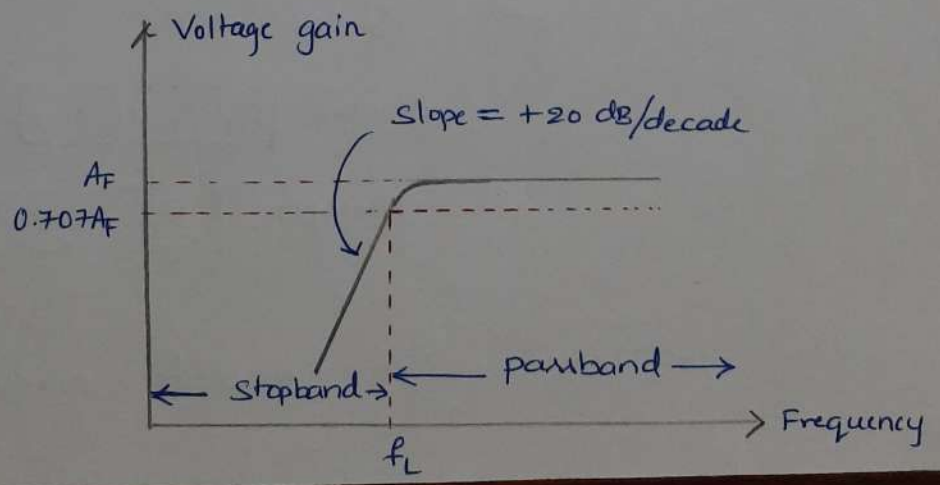
i.e 3 dB down from the level of A_F

3. At $f > f_L$ i.e high frequencies, 1 can be neglected in eqn. (10) as compared to $\left(\frac{f}{f_L}\right)$ in the denominator.

Therefore $\left|\frac{V_o}{V_{in}}\right| = A_F$ i.e Constant

→ For the frequencies, $f < f_L$ the gain increases till $f = f_L$ at a rate of +20 dB/decade.

Hence the slope of the frequency response in stop band is +20 dB/decade for first order high-pass filter



(P) Design a high-pass filter with a cutoff freq. of 10 KHz with a passband gain of 1.5. Also, plot the freq. response for the designed filter.

Solution :

Step 1 : The lower cutoff frequency is 10KHz

i.e $f_L = 10KHz$

Step 2 : Choose C less than $1\mu F$

i.e $C = 0.02\ \mu F$

Step 3 : Calculate R using the formula

$$f_L = \frac{1}{2\pi RC} \quad \text{i.e} \quad 10\times10^{3} = \frac{1}{2\pi R\times0.02\times10^{-6}}$$

$$\Rightarrow \boxed{R = 795.77\ \Omega}$$

Step 4 : passband gain of the filter = $1.5 = A_F$

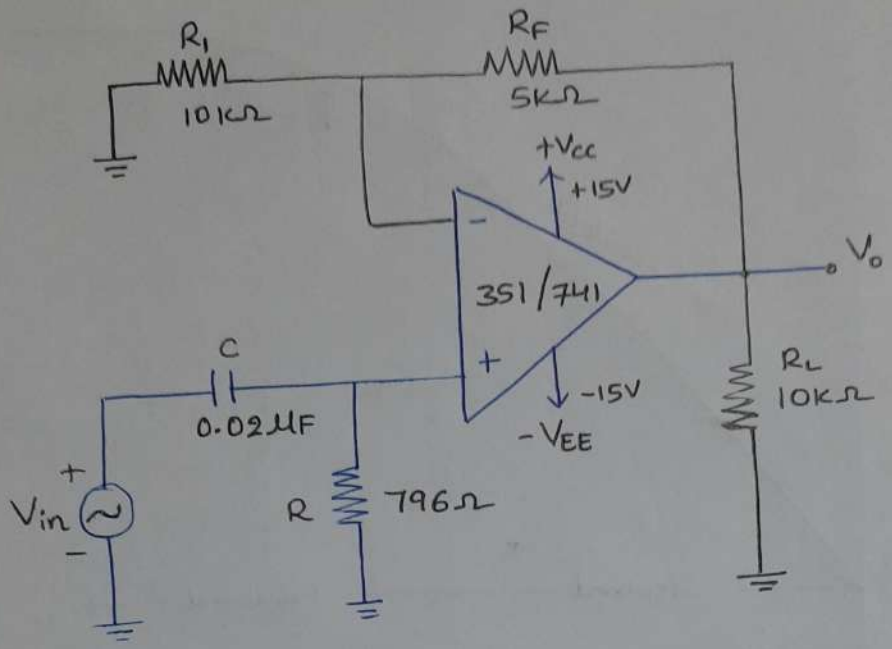
But $A_F = 1 + \frac{R_F}{R_1} = 1.5$

$$\Rightarrow R_F = 0.5\,R_1$$

choose $\boxed{R_1 = 10\,K\Omega}$

Therefore, $\boxed{R_F = 5K\Omega}$

Now, we can write Complete circuit

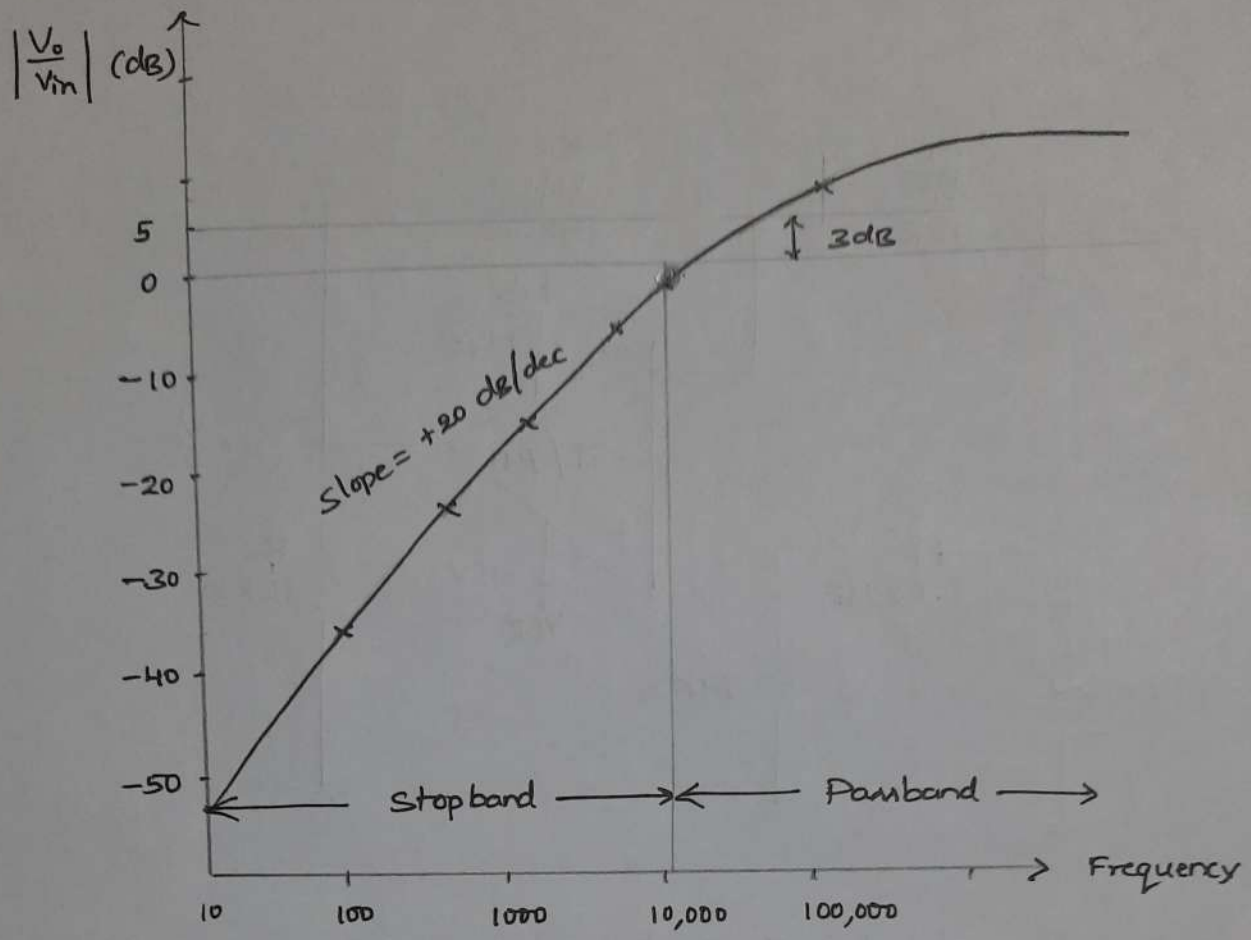


To obtain the frequency response, consider the magnitude of the transfer function of the filter given by

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F\left(\frac{f}{f_L}\right)}{\sqrt{1+\left(\frac{f}{f_L}\right)^2}} = \frac{1.5\left(\frac{f}{10\times10^3}\right)}{\sqrt{1+\left(\frac{f}{10\times10^3}\right)^2}}$$

Now, for various values of f, calculate $\left|\frac{V_o}{V_{in}}\right|$ in dB

f in Hz	$\left\|\frac{V_o}{V_{in}}\right\|$	$\left\|\frac{V_o}{V_{in}}\right\|$ in dB
10	1.5×10^{-3}	−56.48
100	0.015	−36.48
500	0.0749	−22.51
1000	0.149	−16.52
5000	0.671	−3.46
10,000	1.061	0.511
30,000	1.42	3.06
100,000	1.49	3.47



Frequency Response

7.6 Second order High-pass Butterworth Filter

→ The second order high-pass Butterworth filter produces a gain roll-off at the rate of +40 dB/decade in the stop-band

→ This filter can be realised by interchanging the positions of resistors and capacitors in a second order low-pass butterworth filter.

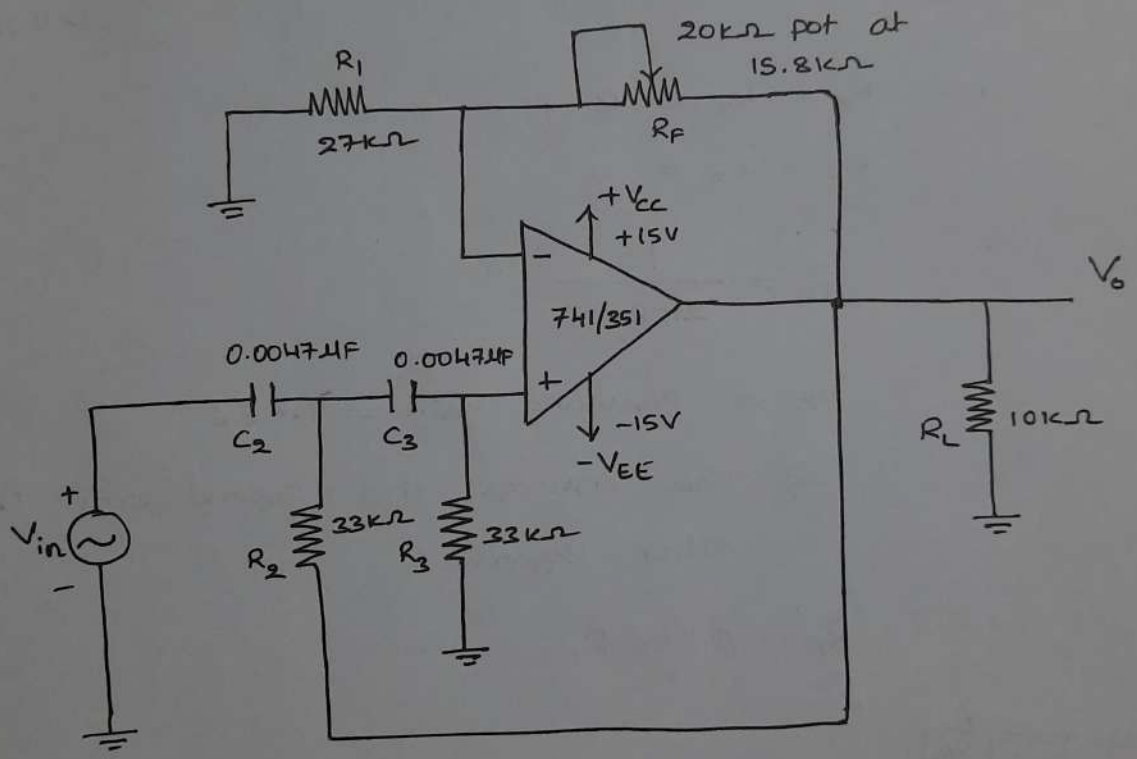


Fig. 1. Second order High-pass Butterworth Filter circuit

→ Fig. 1 shows the second order high-pass Butterworth filter circuit.

→ The analysis and scaling procedures for this filter is exactly same as that of second order low-pass

Butterworth filter.

→ The voltage gain magnitude equation of the second-order high-pass filter is as follows:

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f_L}{f}\right)^4}}$$

where f = Input freq. in Hz

f_L = lower cutoff freq. in Hz $= \frac{1}{2\pi\sqrt{R_2R_3C_2C_3}}$

For $R_2 = R_3 = R$

$C_2 = C_3 = C$

$$f_L = \frac{1}{2\pi RC}$$

A_F = Passband gain = 1.586

⇒ This ensures that second order Butterworth Filter Response

$R_F = 0.586\, R_1$

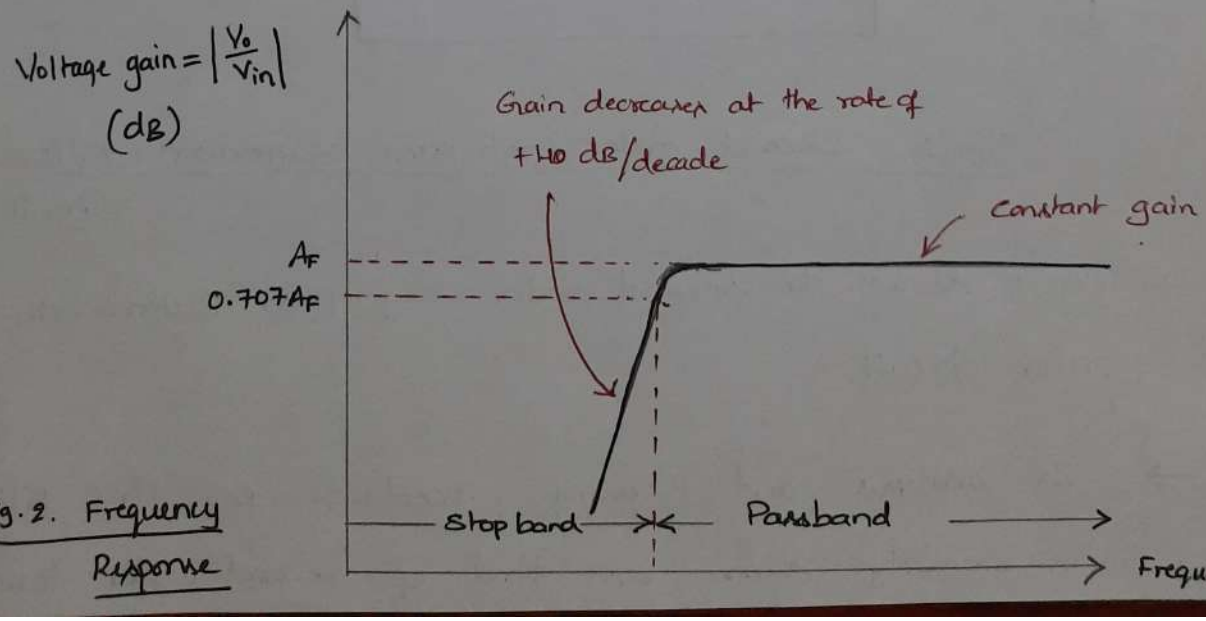
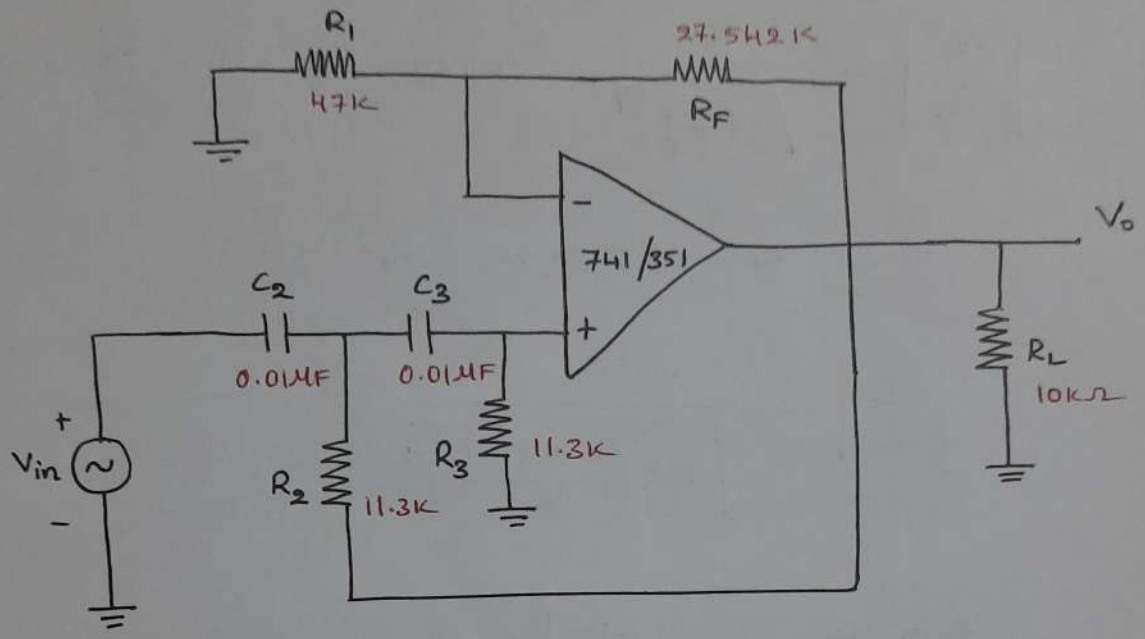


Fig. 2. Frequency Response

(P) For the circuit shown in Fig. a. determine the lower cutoff frequency and then plot the freq. response of the filter. comment on the order of the filter from the freq. response.



Solution: From the circuit diagram

$$R_2 = R_3 = R = 11.3\,K\Omega$$

$$C_2 = C_3 = C = 0.01\,\mu F$$

$$f_L = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}} = \frac{1}{2\pi RC}$$

$$f_L = \frac{1}{(2\pi)(11.3\times10^{3})(0.01\times10^{-6})} = 1.408\,KHz$$

$$\boxed{f_L = 1.408\ KHz}$$

From the two RC section in the circuit, it is clear that the filter is second order high-pass filter

Therefore,

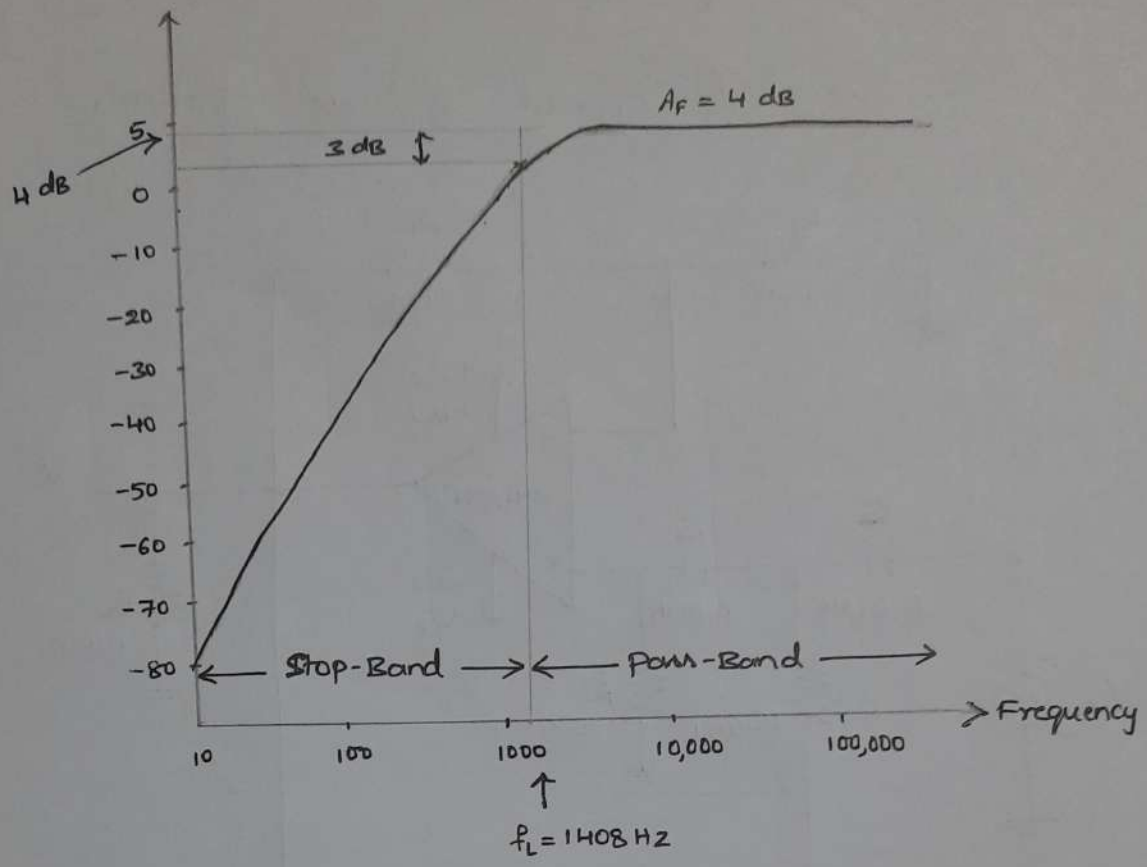
→ To plot the frequency response, let us prepare the table including the gain in dB obtained for various values of input frequency.

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f_L}{f}\right)^4}} \quad \text{where} \quad A_F = 1+\frac{R_F}{R_1} = 1.586$$

since $R_F = 27.542\text{K}\Omega$, $R_1 = 47\text{K}\Omega$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{1.586}{\sqrt{1+\left(\frac{1.4081\text{KHz}}{f}\right)^4}}$$

f in Hz	$\left\|\frac{V_o}{V_{in}}\right\|$	$\left\|\frac{V_o}{V_{in}}\right\|$ in dB
10	8×10^{-5}	−81.93
100	8×10^{-3}	−41.93
500	0.198	−14.04
1000	0.714	−2.93
1408	1.121	0.99
10,000	1.585	4
30,000	1.585	4
100,000	1.586	4



Frequency Response

(P) Design a high-pass second-order filter for the cutoff freq. of 1KHz, pass-band gain, $A_F = 2$.

Solution

Step 1 : lower cutoff freq. $f_L = 1KHz$

Step 2 : choose $C = 0.01\mu F$

Step 3 : $f_L = \frac{1}{2\pi RC}$ Since $R_2 = R_3 = R$

$C_2 = C_3 = C$

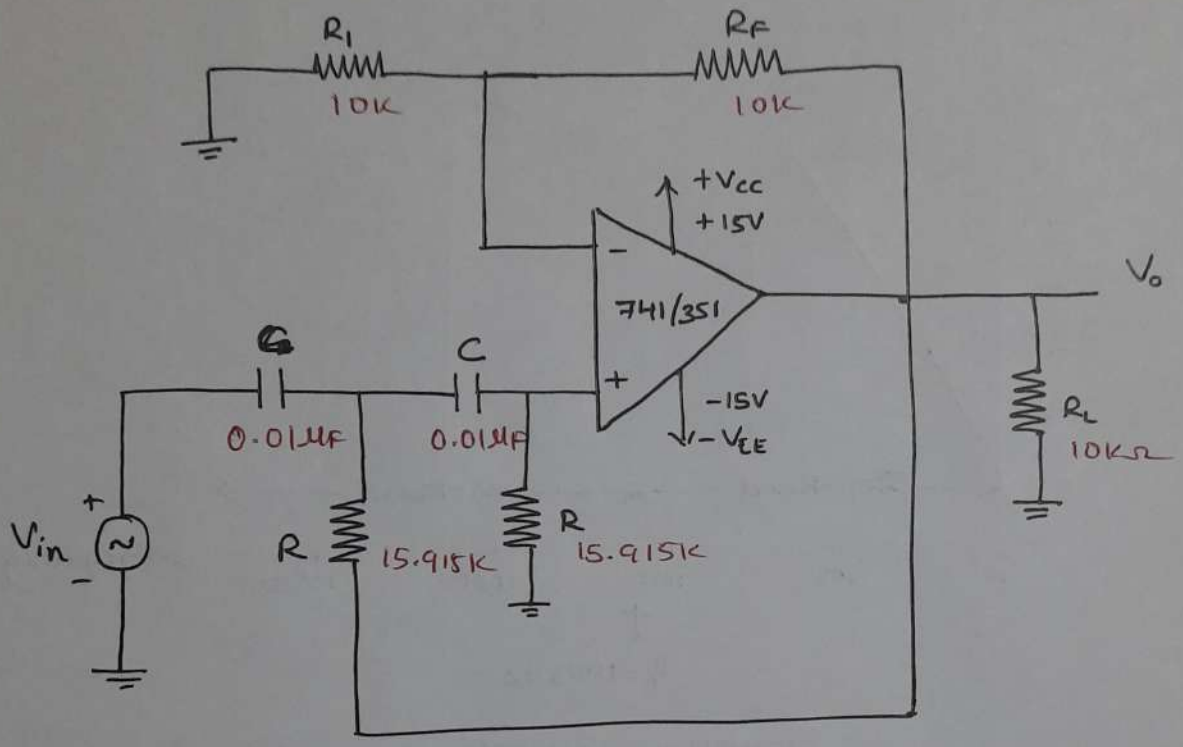
$$R = \frac{1}{2\pi f C} = \frac{1}{(2\pi)(1\times10^{3})(0.01\times10^{-6})}$$

$$\boxed{R = 15.915\ K\Omega}$$

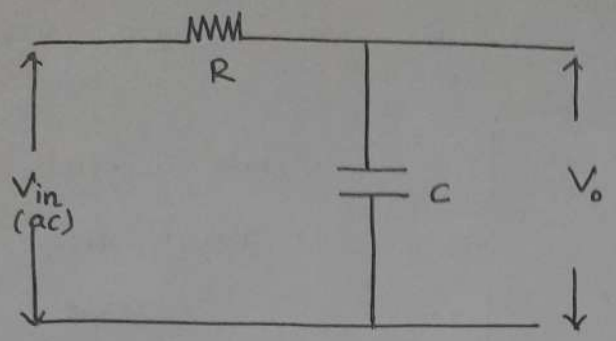
Step 4 : $A_F = 2 \Longrightarrow A_F = 1 + \frac{R_f}{R_1} = 2$

$R_F = R_1 = 10K\Omega$

The designed circuit is as follows:



Low-Pass Filter



This circuit passes low-frequency signals

We know that capacitive reactance X_C is given by

$$X_C = \frac{1}{2\pi fC}$$

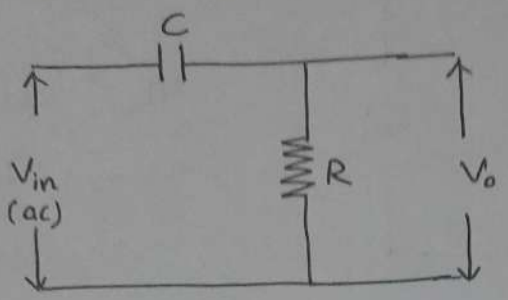
At low frequencies, X_C = High, $V_o = V_{in}$

At high frequencies, X_C = low, $V_o = 0$

Therefore, the RC network shown here works as a low-pass filter.

High-pass Filter

R and C are interchanged



This circuit passes High freq. signals

From Capacitance reactance formula : $X_c = \frac{1}{2\pi f C}$

At low frequencies, X_c = high, Therefore $V_o \neq V_{in}$

At high frequencies X_c = low, Therefore $V_o = V_{in}$

Thus, the RC network shown here will work like a high-pass filter.

→ Therefore, it is clear from our discussion that simple R and C section behaves as a filter.

→ These RC sections are used in active filter along with the active element, Op-amp.

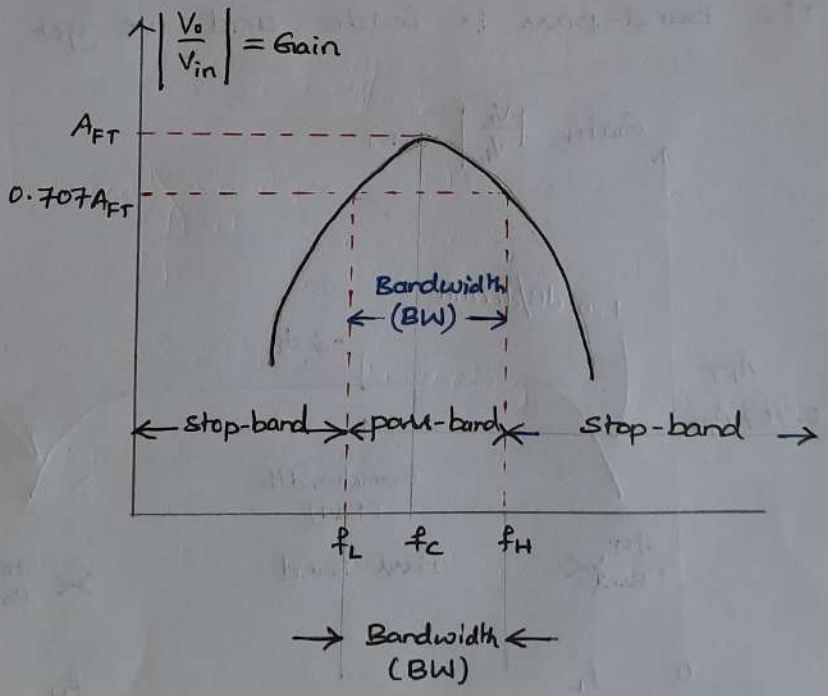
7.8 BAND-PASS FILTERS

Defn: A band-pass filter has a pass-band between two frequencies f_H and f_L such that $f_H > f_L$. Any input freq. outside this pass-band is attenuated.

→ The pass-band between f_H and f_L is called **bandwidth** of the filter denoted as BW

$$BW = f_H - f_L$$

→ The frequency at the centre of the pass-band is called **centre frequency** denoted as f_c. The gain is maximum at f_c and is denoted as A_{FT} called **total pass-band** gain.



→ Practically, the centre frequency, f_c is not exactly at the centre of the pass-band hence it is called as **Resonant Frequency**. The gain at f_L and $f_H = 0.707A_{FT}$

Types of Band-pass Filter

→ Basically, there are two types of band-pass filters which is classified based on the Figure of Merit or Quality Factor (Q)

1. Wide Band-pass Filter
2. Narrow Band-pass Filter

1. Wide Band-pass Filter

→ For Quality factor, $Q < 10$ the band-pass filter is called wide band-pass filter.

→ The band-pass is wide and we get large band-width

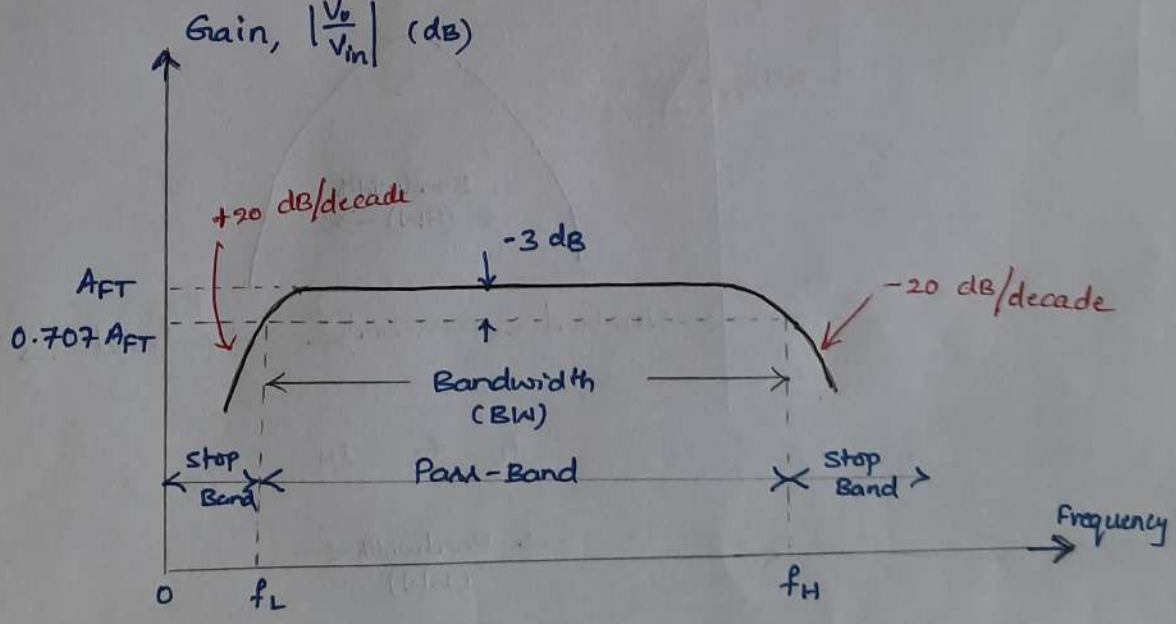


Fig. 1. Frequency Response of Wide Band-pass Filter

2. Narrow Band-pass Filter

→ For $Q > 10$, the bandpass filter is called narrow bandpass filter.

→ The bandpass is very narrow and the bandwidth is very small

→ Higher the value of Q, narrower is the passband and more selective is the filter.

→ In the narrow bandpass filter, the gain peaks at the centre frequency.

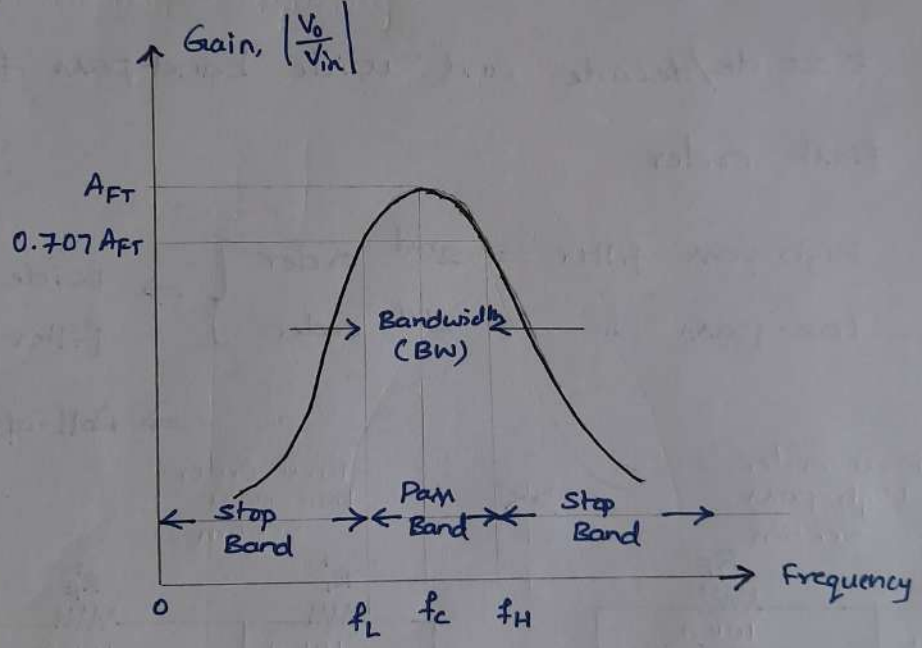


Fig. 2: Frequency Response of Narrow Bandpass Filter

→ For $f < f_L$: Gain roll-off at +20 dB/decade

$f > f_H$: Gain roll-off at −20 dB/decade

→ For wide band-pass filter, the centre frequency is given by

$$f_c = \sqrt{f_L f_H}$$

The relationship between Q and 3-dB bandwidth with f_c is given by

$$Q = \frac{f_c}{BW} = \frac{f_c}{f_H - f_L}$$

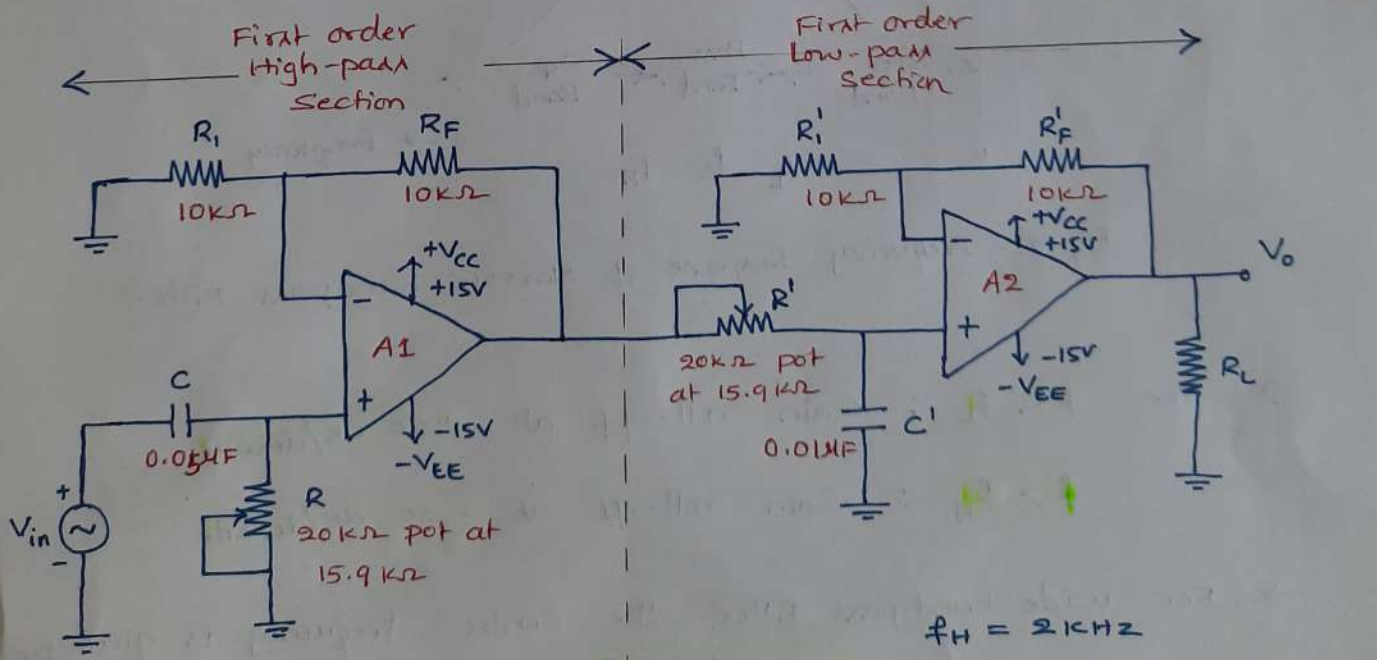
7.8.1 Wide Band-pass Filter

→ The wide band filter can be realised by simply cascading a high-pass filter and low-pass filter.

→ If both high-pass and low-pass filters are of first order, the gain rolls off in both the stop-bands at ± 20 dB/decade and wide band-pass filter is of first order

→ If High-pass filter = 2nd order
Low-pass " = 2nd order
⇒ wide band-pass filter = 2nd order

⇒ Roll-off = ± 40 dB/dec.



f_L = 200Hz

f_H = 2KHz

Fig. 3 Wide Band-pass Filter

→ Fig. 3 shows the first order wide band-pass filter obtained by cascading first order high-pass and low-pass filter sections.

→ The voltage gain expressions for the two sections are reproduced here for the convenience

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f}{f_H}\right)^2}}$$ → First order Low-pass section

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F\left(\frac{f}{f_L}\right)}{\sqrt{1+\left(\frac{f}{f_L}\right)^2}}$$ → First order High-pass section

→ As the two circuits are in cascade, the overall gain of wide band-pass filter is the product of two gains expressed as

$$\boxed{\left|\frac{V_o}{V_{in}}\right| = \frac{A_{FT}\left(\frac{f}{f_L}\right)}{\sqrt{\left[1+\left(\frac{f}{f_L}\right)^2\right]\left[1+\left(\frac{f}{f_H}\right)^2\right]}}}$$

where A_{FT} = Total pass-band gain

f = Input frequency in Hz

f_L = Lower cutoff frequency in Hz

f_H = Higher cutoff frequency in Hz.

and $\boxed{A_{FT} = A_1 A_2}$

where A_1 = Gain of high-pass section

A_2 = Gain of low-pass section

7.8.2. Narrow Band-pass Filter

The narrow band-pass filter uses only one-opamp as against two by wide band-pass filter:

(i) It uses two feedback paths (Multiple Feedback)

(ii) The op-amp is in Inverting configuration

Due to two feedback paths, the narrow bandpass filter is called Multiple feedback filter.

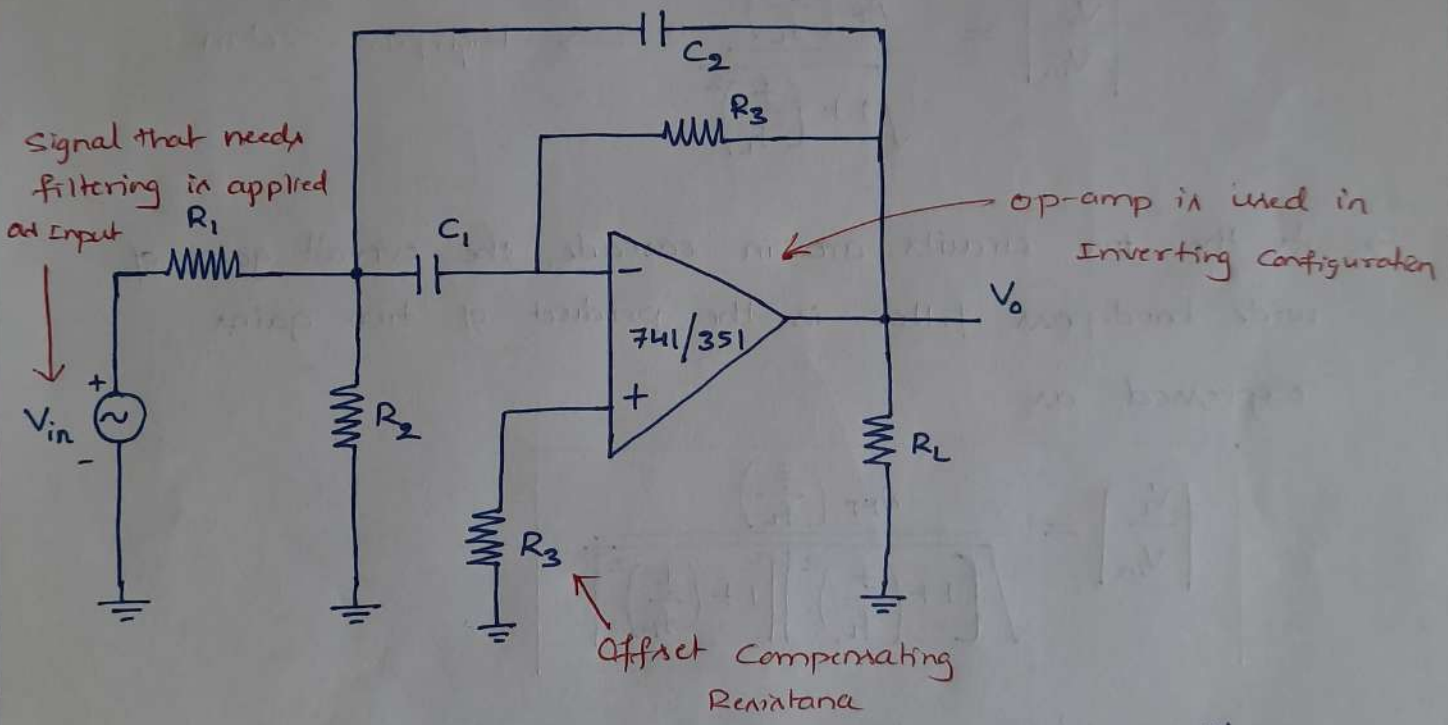


Fig. 4. Multiple-Feedback Narrow Band-pass Filter

→ Fig. 4 shows the circuit diagram of narrow band-pass filter. Circuit.

→ Op-amp is used in Inverting Configuration.

→ The resistance R_3 connected to non-inverting input terminal is offset compensating resistance

→ The important parameters of the narrow band-pass filter are : f_L, f_H, the centre frequency f_c, the gain at the centre frequency A_F and the quality factor Q.

→ The relationship of components with the various parameters are given by the following.

For simplifying calculations, choose $C_1 = C_2 = C$

$$R_1 = \frac{Q}{2\pi f_c C A_F} \quad \text{——(1)}$$

$$R_2 = \frac{Q}{2\pi f_c C (2Q^2 - A_F)} \quad \text{——(2)}$$

$$R_3 = \frac{Q}{\pi f_c C} \quad \text{——(3)}$$

and $A_F = \frac{R_3}{2R_1}$ → Gain at f_c ——(4)

The gain A_F must satisfy the equation

$$A_F < 2Q^2 \quad \text{——(5)}$$

changing the centre frequency f_c :

let f_c = original frequency

f_c' = New centre frequency

The new centre frequency can be achieved by

changing the resistance, R_2.

The new value of resistance say R_2' can be obtained as : $R_2' = R_2\left(\frac{f_c}{f_c'}\right)^2$

Example : Design a wide band-pass filter having $f_L = 400\,Hz$ and $f_H = 2\,KHz$ and pass band gain of 4. Draw the frequency response of the filter and also calculate the Q value of the filter.

Solution : ↯ Design the low-pass filter with $f_H = 2KHz$

let $C' = 0.01\,\mu F$

$$f_H = \frac{1}{2\pi R'C'}$$

$$i.e \quad R' = \frac{1}{2\pi \times 2\times10^{3} \times 0.01\times10^{-6}} = 7.957\,K\Omega$$

$$\boxed{R' = 7.957\,K\Omega}$$

↯ Design the high-pass filter with $f_L = 400\,Hz$

let $C = 0.05\,\mu F$

$$f_L = \frac{1}{2\pi RC} \quad i.e \quad R = \frac{1}{2\pi f C}$$

$$R = \frac{1}{2\pi \times 400 \times 0.05 \times10^{-6}} = 7.95\,K\Omega$$

$$\boxed{R = 7.95\,K\Omega}$$

Now $A_{FT} = A_1 A_2$

where A_1 = Gain of the high-pass section, and

A_2 = Gain of the low-pass section

A_{FT} is given as 4 = Total pass-band gain

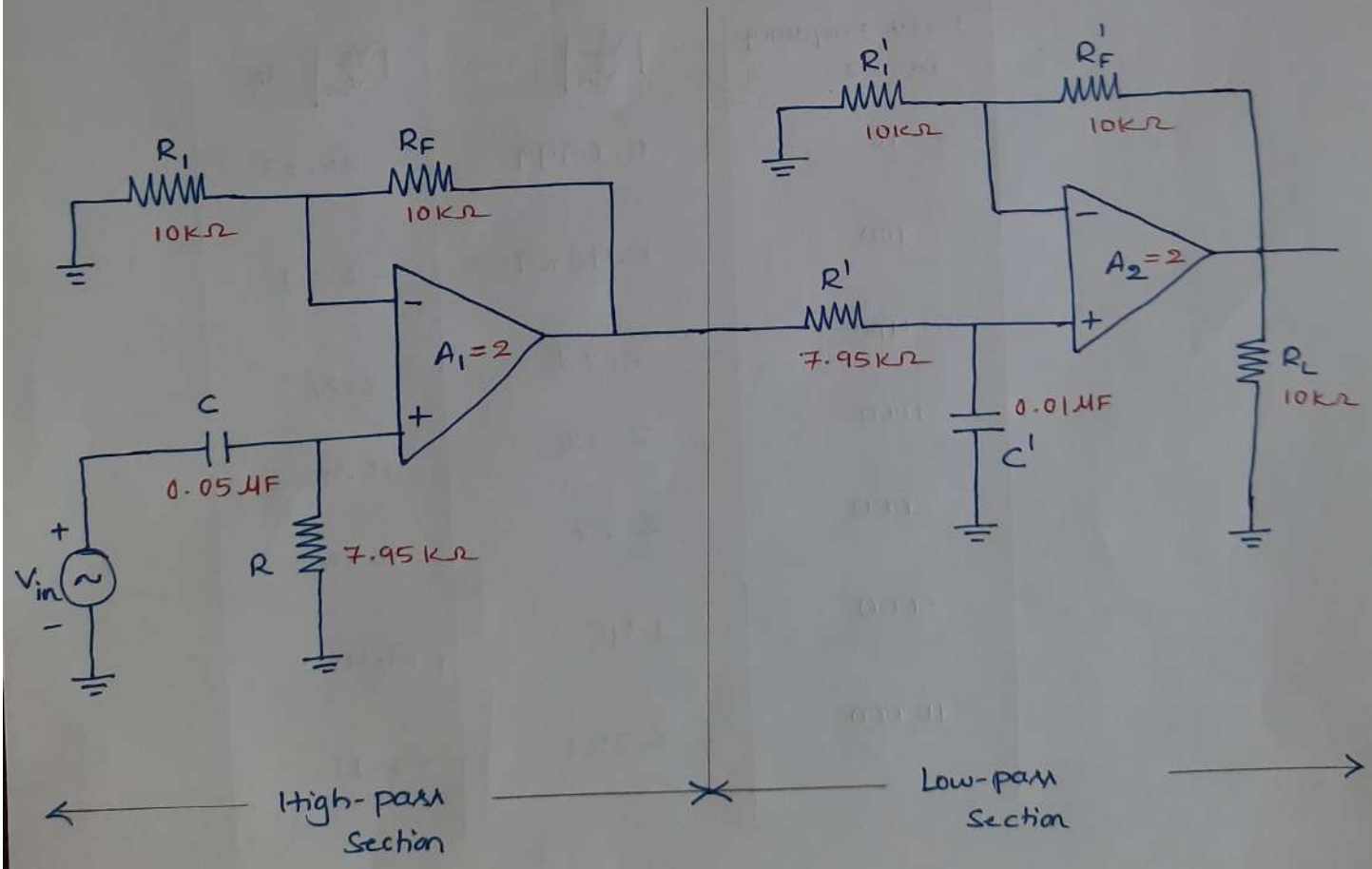
let $A_1 = A_2 = 2$

Now for the non-inverting op-amp

$$A_1 = A_2 = 1 + \frac{R_F}{R_1} = 2$$

For Both the sections, let $R_F = R_1 = 10\,K\Omega$

Hence the designed circuit is as shown in Fig. 5



To obtain the frequency response, overall gain equation is used

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_{FT}\left(\frac{f}{f_L}\right)}{\sqrt{\left[1+\left(\frac{f}{f_L}\right)^2\right]\left[1+\left(\frac{f}{f_H}\right)^2\right]}}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{4\left(\frac{f}{400}\right)}{\sqrt{\left[1+\left(\frac{f}{400}\right)^2\right]\left[1+\left(\frac{f}{2\times10^3}\right)^2\right]}}$$

Now, select the frequencies and tabulate the data for the frequency response

Input Frequency in Hz	$\left\|\frac{V_o}{V_{in}}\right\|$	$\left\|\frac{V_o}{V_{in}}\right\|$ dB
10	0.0999	−20.27
100	0.9689	−0.27
400	2.77	8.86
1000	3.32	10.42
2000	2.77	8.86
5000	1.48	3.41
10,000	0.783	−2.11

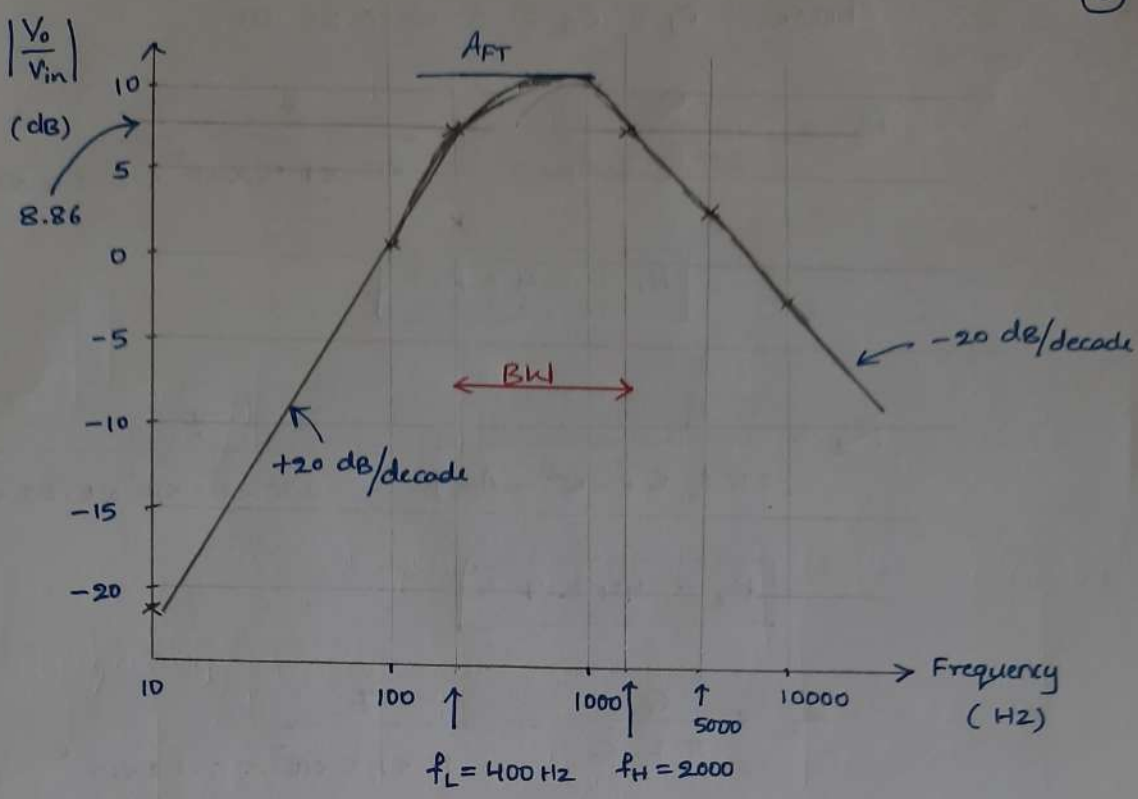


Fig. Frequency Response

Now $f_c = \sqrt{f_L f_H} = \sqrt{400 \times 2000} = 894.427$ Hz

$BW = f_H - f_L = 2000 - 400 = 1600$ Hz

$$Q = \frac{f_c}{BW} = \frac{894.427}{1600} = 0.559$$

Thus Q is less than 10, for wide Bandpass Filter.

Example: Design the Narrow bandpass filter with two feedback paths with $f_c = 1.5$ KHz, $Q = 7$ and $A_F = 15$. Calculate new value of the resistance in the circuit which will change f_c to 2KHz.

Choose $C_1 = C_2 = C = 0.02\ \mu F$

$$R_1 = \frac{Q}{2\pi f_c C A_F} = \frac{7}{2\pi \times 1.5 \times 10^3 \times 0.02 \times 10^{-6} \times 15}$$

$$\boxed{R_1 = 2.47\ K\Omega}$$

$$R_2 = \frac{Q}{2\pi f_c C (2Q^2 - A_F)} = \frac{7}{2\pi \times 1.5 \times 10^3 \times 0.02 \times 10^{-6} (2 \times 7^2 - 15)}$$

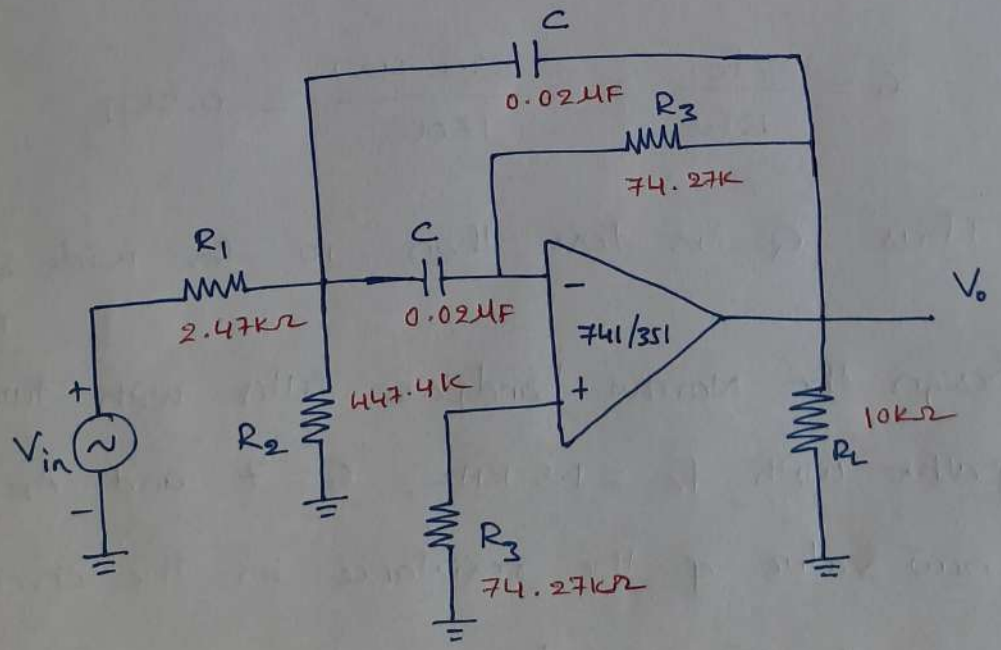
$$\boxed{R_2 = 447.4\ \Omega}$$

$$R_3 = \frac{Q}{\pi f_c C} = \frac{7}{\pi \times 1.5 \times 10^2 \times 0.02 \times 10^{-6}}$$

$$\boxed{R_3 = 74.27 K\Omega}$$

The resistance R_2 can changed to get R_2' = at $f_c = 2KHz$

$$R_2' = R_2 \left(\frac{f_c}{f_c'}\right)^2 = 447.4\Omega \times \left(\frac{1.5}{2}\right)^2 = 251.66$$



Homework Problems

1. Design a wide band pass filter with $f_L = 200$ Hz, $f_H = 1$ KHz and a passband gain = 4. Draw the frequency response plot of this filter. Calculate the value of Q for the filter. Soln: R = 15.9 KΩ for C = 0.05 μF
   Q = 0.56

2. Design a bandpass filter with multiple feedback paths having $f_c = 1$ KHz, $Q = 3$, and $A_F = 10$. change the centre frequency to 1.5 KHz, keeping A_F and the bandwidth constant. Sol: For $C_1 = C_2 = C = 0.01\,\mu F$
   $R_1 = 4.77\,K\Omega$, $R_2 = 5.97\,K\Omega$
   $R_3 = 95.5\,K\Omega$, $R_2' = 2.65\,K\Omega$

Summary

→ Introduced band-pass filter and discussed on various types of band-pass filters namely,
- wide band-pass filter ($Q < 10$)
- Narrow band-pass filter ($Q > 10$)

→ Discussion on the implementation of these two types of band pass filter.

→ Worked out few examples to understand the design aspects discussed.

UNIT 8

555 Timer

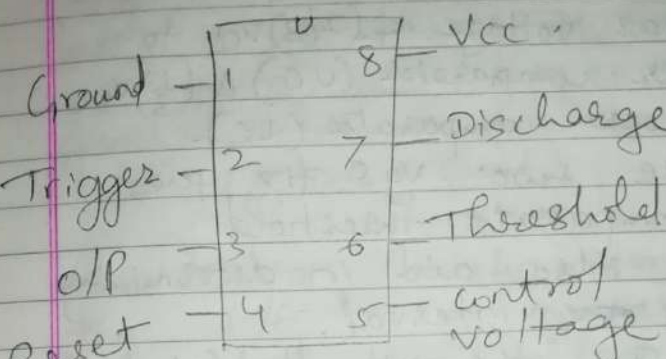
A 555 timer is a highly stable device for generating accurate time delay or oscillation. A single 555 timer can provide time delay ranging from micro seconds to hours. ~~counter timer can have a max timing range of days.~~

- Supply Vg range: +5V to +18V
- Can drive load up to 200mA
- Compatible with both TTL and CMOS logic circuits.

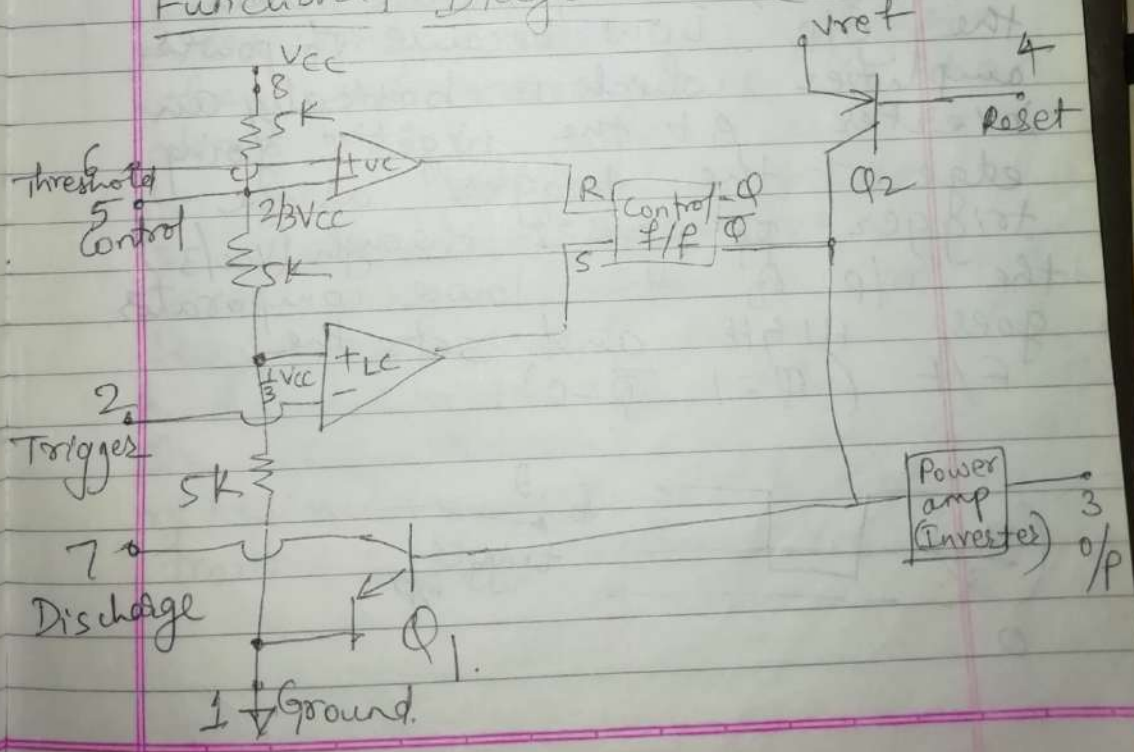
Applications:

Oscillator, pulse generator, ramp and square wave generator, mono-shot multivibrator, burglar alarm, traffic light control and voltage monitor etc.

(2) Pin diagram (8 pin mini DIP)



Functional Diagram (1000) Dec 09

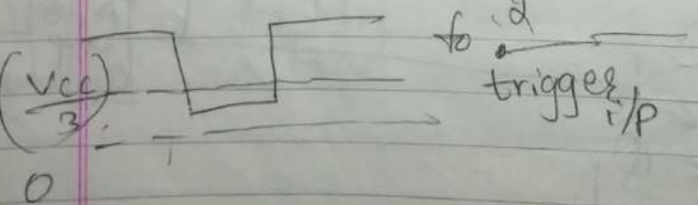


Teacher's Signature .....

(3)

The three 5 kΩ internal resistors act as voltage dividers, providing bias voltage of $(2/3)V_{CC}$ to the upper comparator (UC) & $(\frac{1}{3})V_{CC}$ to the lower comparator (LC). Since these two Vgs fix the necessary comparator threshold vg, they also aid in determining the timing ~~red~~ interval.

In the standby (stable) state the o/p $\overline{Q}$ of the control f/f (FF) is HIGH. This makes the o/p LOW because of power amplifier which is basically an inverter. At the negative going edge of the trigger as the trigger ~~pp~~ passes through $(V_{CC}/3)$ the o/p of the lower comparator goes HIGH and sets the f/f ($Q=1$ $\overline{Q}=0$).



(4)

(4)

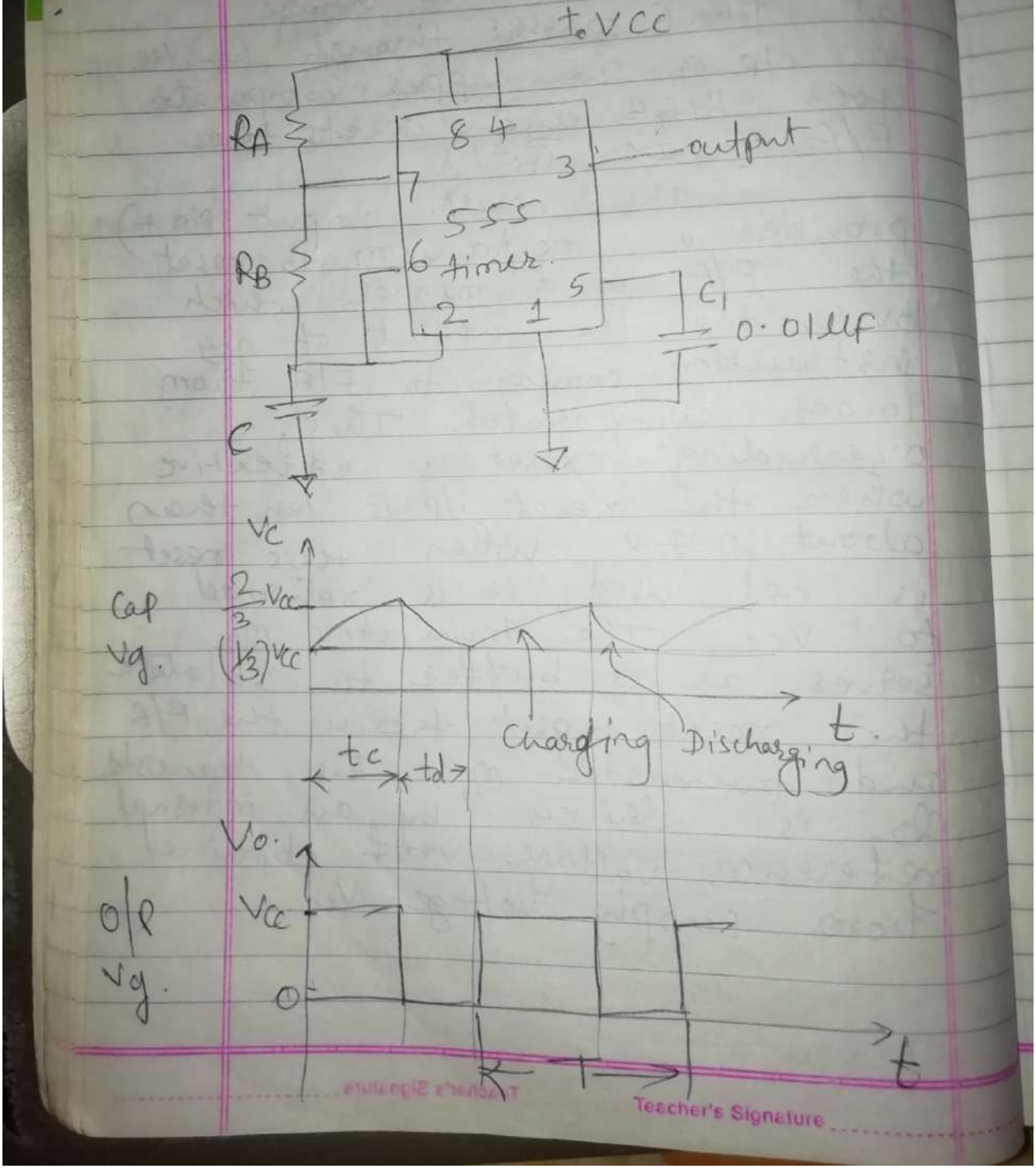
During the positive excursion, when the threshold voltage at pin 6 passes through $(\frac{2}{3})V_{CC}$, the o/p of the upper comparator goes HIGH and resets the F/F ($Q=0$, $\overline{Q}=1$).

The reset input (pin 4) provides a mechanism to reset the F/F in a manner which overrides the effect of any instruction coming to F/F from lower comparator. This overriding reset is effective when the reset i/p is less than about 0.4 V. When this reset is not used, it is returned to V_{CC}. The transistor Q_2 serves as a buffer to isolate the reset input from the F/F. and transistor Q_1. The transistor Q_2 is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{CC}.

Teacher's Signature .....

(5)

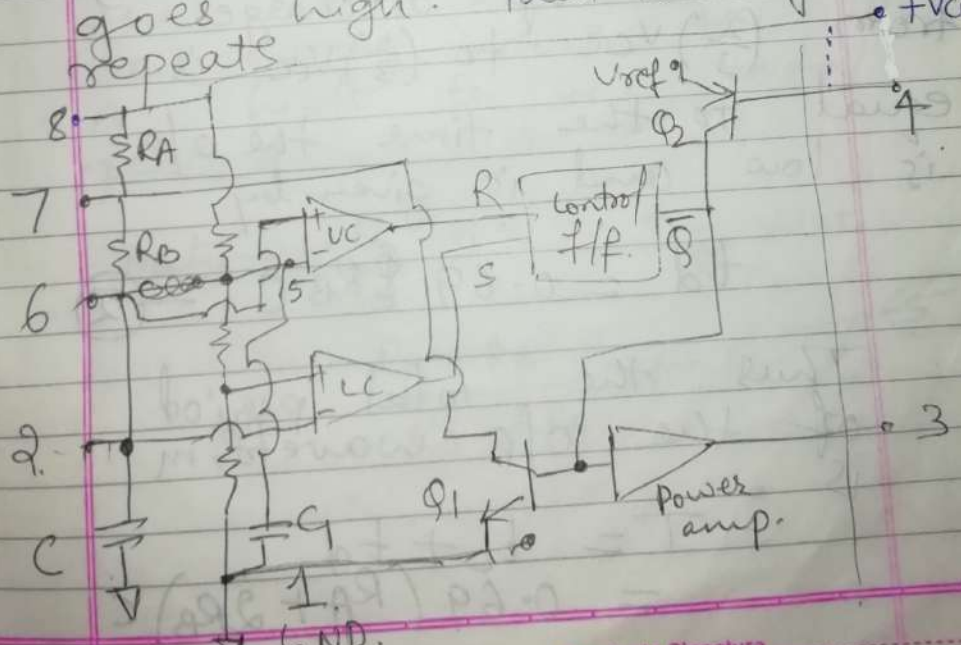
Astable Multivibrator



(6)

Initially, when the output is high, capacitor C starts charging toward Vcc thro' RA and RB.

When the vg across the capacitor equals $\left(\frac{2}{3}\right)$Vcc comparator 1 (UC) triggers the f/f and o/p switches LOW. Now capacitor C starts discharging through RB and transistor Q_1 when the voltage across C equals $\left(\frac{1}{3}\right)$Vcc, the lower comparators output triggers the f/f and the output goes high. Then the cycle repeats.



Teacher's Signature .....

(7)

As shown in the fig the capacitor is periodically charged and discharged between $(2/3)V_{CC}$ and $(\frac{1}{3})V_{CC}$ respectively. The time during which the capacitor charges from $(\frac{1}{3})V_{CC}$ to $(\frac{2}{3})V_{CC}$ is equal to the time the o/p is high and is given by

$$t_c = 0.69(R_A + R_B)C \quad \text{—(1)}$$

Similarly the time during which the cap discharges from $(\frac{2}{3})V_{CC}$ to $(\frac{1}{3})V_{CC}$ is equal to the time the o/p is low and is given by

$$t_d = 0.69 R_B C \quad \text{—(2)}$$

Thus the total period of the o/p waveform is

$$T = t_c + t_d$$
$$= 0.69(R_A + 2R_B)C$$

Teacher's Signature

(3)

(8)

(8) This in turn gives the frequency of oscillation as

$$f_o = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \quad \text{——— (4)}$$

Eqn (4) indicates that the freq f_o is independent of supply ug V_{cc}. This freq is called free running freq.

Duty cycle is defined as the ratio of the on time t_c during which the o/p is high to the total period T.

$$\text{Duty cycle in \%} = D = \frac{t_c}{T} \times 100. \quad \text{——— (5)}$$

$$= \frac{R_A + R_B}{R_A + 2R_B} \times 100.$$

Teacher's Signature

(9)

Q4

Astable MV

The capacitor voltage for a low pass RC ckt subjected to a step i/p of Vcc volts is given by

$$v_c = V_{cc}\left(1 - e^{-t/RC}\right)$$

~~At t=0~~, the time t_1 taken by the ckt to change from 0 to $(2/3)V_{cc}$ is

$$\frac{2}{3}V_{cc} = V_{cc}\left(1 - e^{-t_1/RC}\right)$$

$$t_1 = 1.09\,RC \quad \text{---(1)}$$

Now the time t_2 to charge from 0 to $(\frac{1}{3})V_{cc}$ is

$$\left(\frac{1}{3}\right)V_{cc} = V_{cc}\left(1 - e^{-t_2/RC}\right)$$

$$t_2 = 0.405\,RC \quad \text{---(2)}$$

So the time to charge from $\frac{1}{3}V_{cc}$ to $\frac{2}{3}V_{cc}$ is

$$t_{high} = t_1 - t_2$$

(96)

$= 1.09RC - 0.405RC$

$= 0.69RC$

So for the given ckt

$t_{high} = 0.69(R_A + R_B)C$ — (3)

The o/p is low while the capacitor discharges from $(\frac{2}{3})V_{CC}$ to $(\frac{1}{3})V_{CC}$ and the v_g across the capacitor is given by

$(\frac{1}{3})V_{CC} = (\frac{2}{3})V_{CC}\, e^{-t/RC}$

upon solving we get

$t = 0.69RC$

For the given ckt

$t_{low} = 0.69\, R_B C.$ — (4)

Teacher's Signature

RC (10)

Ex Given $R_A = 6.8\,K\Omega$

$R_B = 3.3\,K\Omega$

$C = 0.1\,\mu F$

Calculate

(a) t_{HIGH} & t_C

(b) t_{LOW} & t_d.

(c) free running frequency f_0

(d) Duty cycle D.

Soln

$t_C = 0.69\,(R_A + R_B)\,C.$

$= 0.69\,(6.8 + 3.3)\,10^{3} \times 0.1 \times 10^{-6}$

$= 0.6969$ msec.

$\simeq 0.7$ msec

$t_d = 0.69\,R_B\,C.$

$= 0.69 \times 3.3 \times 10^{3} \times 0.1 \times 10^{-6}$

$= 0.2277$ msec

$\simeq 0.23$ msec

Teacher's Signature

(11)

(c) $f_o = \frac{1}{T}$

$= \frac{1}{t_c + t_d} = 1.0779\,kHz$

(d) $D = \frac{t_c}{T} \times 100$

$= 75.455\,\%$

Ex Lay K. For astable MV $R_A = 2.2k\Omega$ $R_B = 3.9k\Omega$ $C = 0.1\mu F$. Determine the +ve pulse width t_c, -ve Pulse width t_d free running freq f_o & Duty cycle

Ans $t_c = 0.421\,ms$.
$t_d = 0.269\,ms$
$f_o = 1.45\,kH$.
$D = 61.045\,\%$.

Teacher's Signature .....

(12)

Ex A 555 astable MV has $R_A = 2.2\,k\Omega$, $R_B = 6.8\,k\Omega$, $C = 0.01\,\mu F$

June 08 (07m)

cal (a) t_{high} (b) t_{low} (c) f_o (d) Duty cycle

Draw the connection diagram

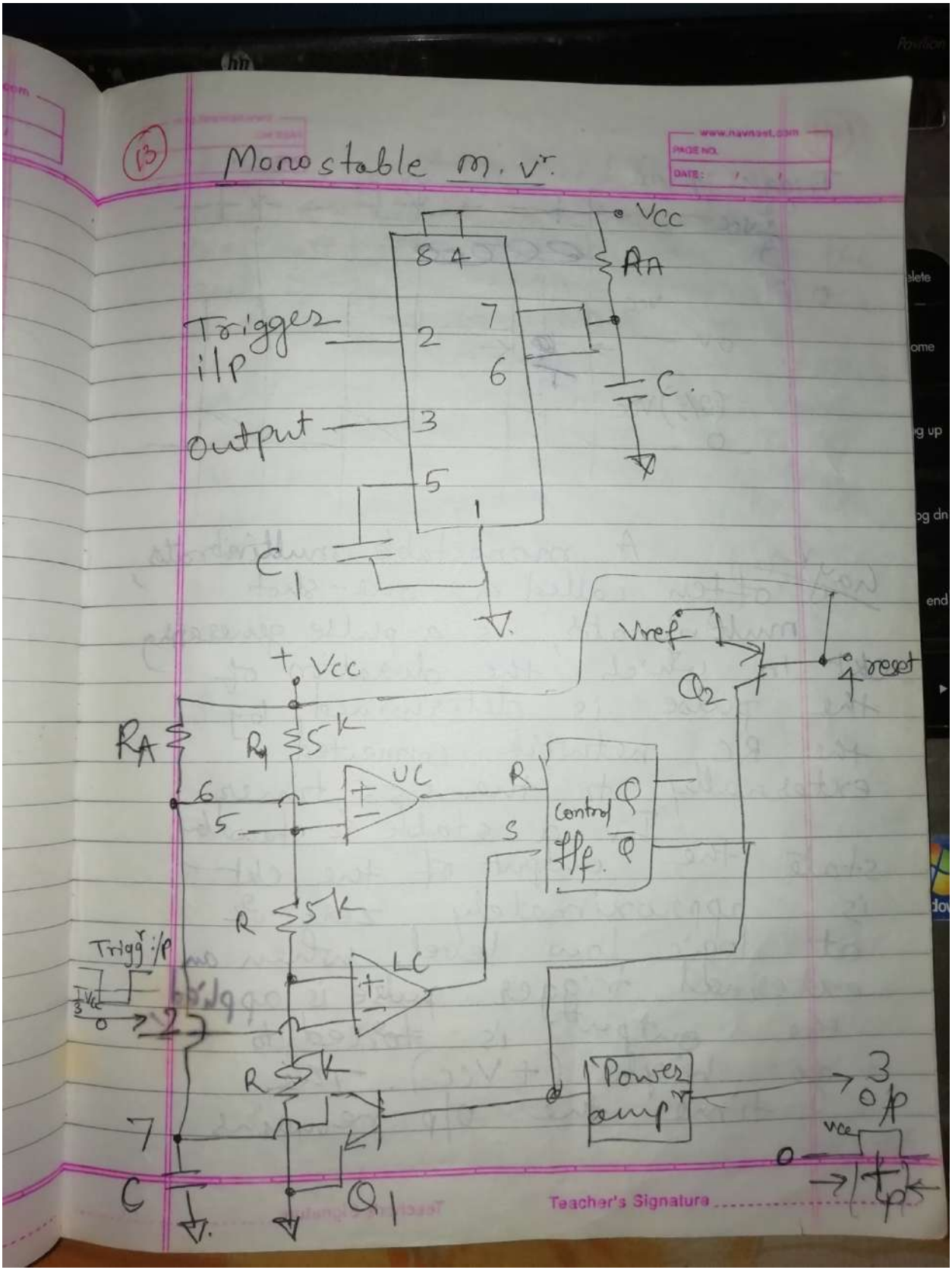
$t_{high} = 62.1\,\mu sec$

$t_{low} = 46.92\,\mu sec$

$f_o = 9.173\,kHz$

$D = 56.96\,\%$

Teacher's Signature .....


13
Monostable m.v.r.
Vcc
RA
8
4
7
2
6
3
5
1
Trigger i/p
output
C.
C1
Vref
reset
Q2
+ Vcc
RA
R
5K
6
5
UC
R
S
Control ff.
Q
R
5K
Trigg i/p
1/3 Vcc
0
LC
R
5K
Power amp
3
o/p
Vcc
7
C
Q1
Teacher's Signature

A monostable multivibrator, often called a one-shot multivibrator, is a pulse generating ckt in which the duration of the pulse is determined by the RC network connected externally to the 555 timer.

In a stable or standby state the output of the ckt is approximately zero or at logic low level. When an external trigger pulse is applied the output is forced to go high (+Vcc). The time the o/p remains

(15)

high is determined by the external RC network connected to the timer. At the end of the timing interval the output automatically reverts back to its logic low-stable state. The output stays low until the trigger pulse is again applied. Then the cycle repeats. The monostable ckt has only one stable state (o/p low) hence the name monostable.

Operation

Initially when the o/p is low, ie the ckt is in a stable state, transistor Q_1 is on and capacitor C is shorted out to ground. However, upon application of a negative trigger pulse to pin 2, transistor Q_1 is turned off which releases the short ckt across the external capacitor and drives

Teacher's Signature .....

the o/p high. The capacitor C now starts charging up toward Vcc through RA. However, when the voltage across the capacitor equals $\left(\frac{2}{3}\right)V_{CC}$, ~~comp~~ upper comparator's output switches from low to high, which in turn drives the output to its low state via the output of the control f/f. At the same time the output of the f/f turns on the Q_1 transistor and hence capacitor C rapidly discharges through the transistor. The output of the monostable remains low until a trigger pulse is again applied. Then the cycle repeats.

The pulse width of the output or the time during which the o/p remains high is given by

$$t_p = 1.1 R_A C$$

Derivation last page (P) ✓✓

Ex for MS MVR

$R_A = 10\ k\Omega$

$t_p = 10\ ms$

Det C.

$$C = \frac{t_p}{1 R_A} = \frac{10 \times 10^{-3}}{1.1 \times 10 \times 10^3}$$

$$= 0.909\ \mu F$$

$$\simeq 1\ \mu f.$$

Ex RC

$R = 100\ k\Omega$

$T = 100\ ms$

Cal C.

$C = 0.9\ \mu F.$

Teacher's Signature .....

(18)

Monostable multivibrator

The v_c across the capacitor is given by

$$v_c = V_{cc}\left(1 - e^{-t/RC}\right)$$

At $t = T$

$$v_c = \left(\frac{2}{3}\right) V_{cc}$$

$$\therefore \left(\frac{2}{3}\right) V_{cc} = V_{cc}\left(1 - e^{-T/RC}\right)$$

$$\& \quad e^{-T/RC} = 1 - \frac{2}{3} = 1/3$$

$$= 0.333$$

$$-\frac{T}{RC} = \ln 0.333$$

$$= -1.0986$$

$$\frac{T}{RC} = 1.0986$$

$$\simeq 1.1$$

$$\therefore T = 1.1\,RC \text{ sec} \;//$$

Teacher's Signature .....